A Video Generator

(Un Generatore Video)

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Description

The idea to develop a video generator is threefold: the project represents a base to have data output in TV format for microprocessor based instruments; formally it allows to determine the maximum number of vertical lines a TV monitor is able to reproduce and for such reason is able to give an estimation of the spatial resolution; it could be considered an evolute example of using field programmable devices for didattic purposes.

In order to evaluate the resolution feature of a monitor, a pattern of vertical lines is generated in groups, covering the range from 100 to 800 in step of 100 lines if seen in a full screen. Such pattern is able to give quick idea of the resolution capability of the full system under evaluation, including electronics and display.

The system is very compact because all the functionality to produce the pattern and the synchronization signal is realized with a single programmable chip, while the standard video signal levels are obtained with a second dedicated encoder chip.

The project is presented with the PAL encoding scheme, but can easily be converted in NTSC or any computer monitor standard following the same logic. Moreover the pattern generated can be modified or fully changed only using programming modifications.

In fig. 1 a general overview is presented showing the functional parts. The heart of the system is the FPGA chip XC4013, that allows to generate all the synchronization signals and to keep in its internal ROM the pattern to produce as image. This chip is a re-programmable type and the hardware realized is defined by a software configuration contained in the external serial prom XC17256. Then the hardware can be easily modified and different solution can be inserted in the same environment. In the case we are describing, for example the PAL standard can be changed in NTSC standard or any other video combination of synchronization signals and video pattern having as only constrain the maximum number of internal block or, in other words, the maximum number of gates as allowed by the chip. In the system we are discussing of, this number is about 13K gates. The third chip, the AD720JP is used to generate from the RGB and synchronization components, the composite and Y/C signals as the PAL or NTSC standards require.

The description has to go inside the FPGA chip. Three fundamental parts are generated as shown in the fig. 2: the sequencer, the synchronization signal generator and the video pattern generator.

The sequencer produces timing in step of 400 ns for synchronization generation, while video signal produced presents a resolution of 25 ns. A 40 MHz clock is fed into the FPGA and scaled in order to generate a 2.5 MHz clock able to generate a sequence of start and stop pulses. These produce enable status for three counters that are used in sequence. The first drives a prom containing the pattern able to generate the vertical synchronization including pre- and post-equalizing pulses. The second drives iteratively a prom containing the pattern of the horizontal synchronization signals.

The third is used to generate a pattern similar to the first, but with the difference able to produce the interlaced sequence. The continuos running of them produces the vertical and horizontal synchronization signal.

The last block of the FPGA chip we describe, the video pattern generator, uses the direct 40 MHz clock to run a counter that drives a prom containing the pattern we want to show as line. Prom content represent a 1 status for pixel on and 0 for off. A sequence of such states produces lines

large in the left side of the screen and the gradually shorter up to very short. Such pattern is fed as common signal for RGB components in order to produce a black and white image.

Programming in different way the synchronization section is possible to generate NTSC standard, while a different pattern can be shown as line content if required. The choice of NTSC must be reflected in the video encoder selection as the mode pin status and in the clock frequency (NTSC 14.318180 MHz, PAL 17.734.480 MHz). A colored pattern can be generated using different content of the video pattern prom in the different RGB components, having as limitation the maximum number of different states allowed in the FPGA chip and the bandwidth of the crominance component.

The FPGA programming file for the PAL standard can be requested to the author, as the complete set of drawing files.

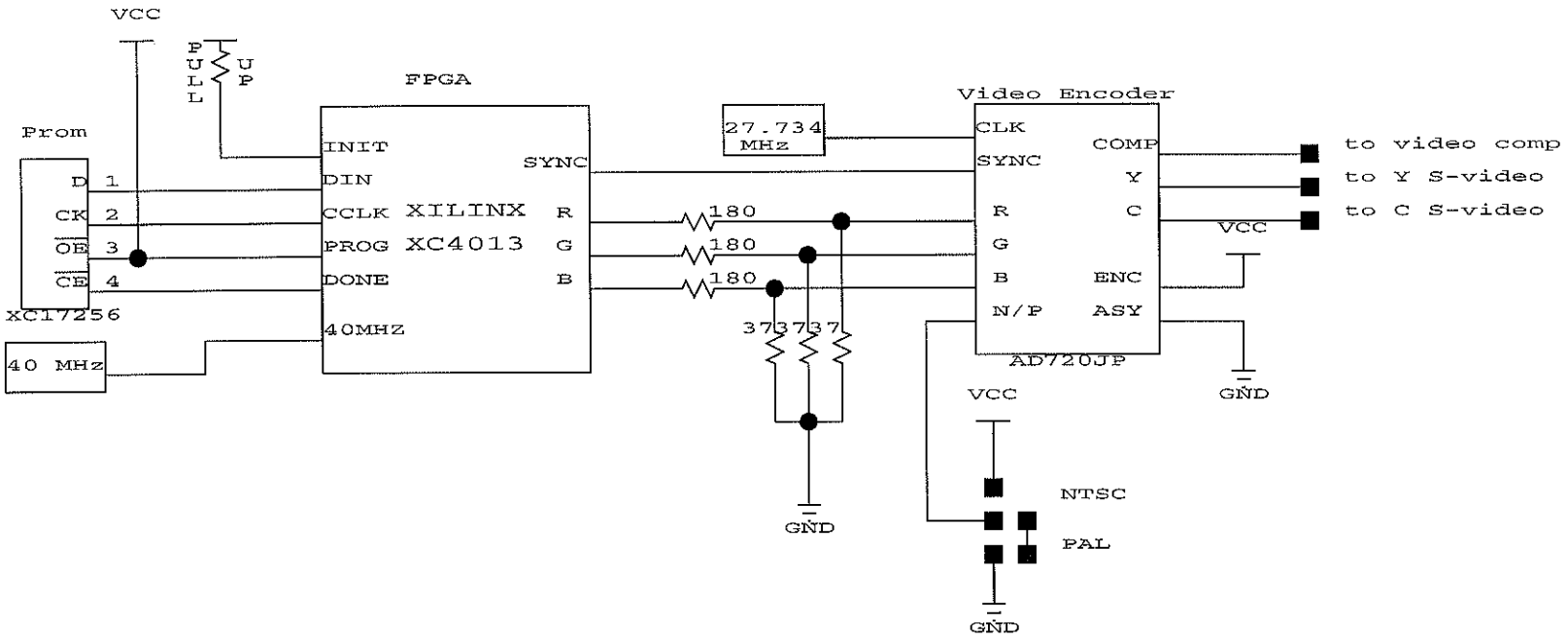
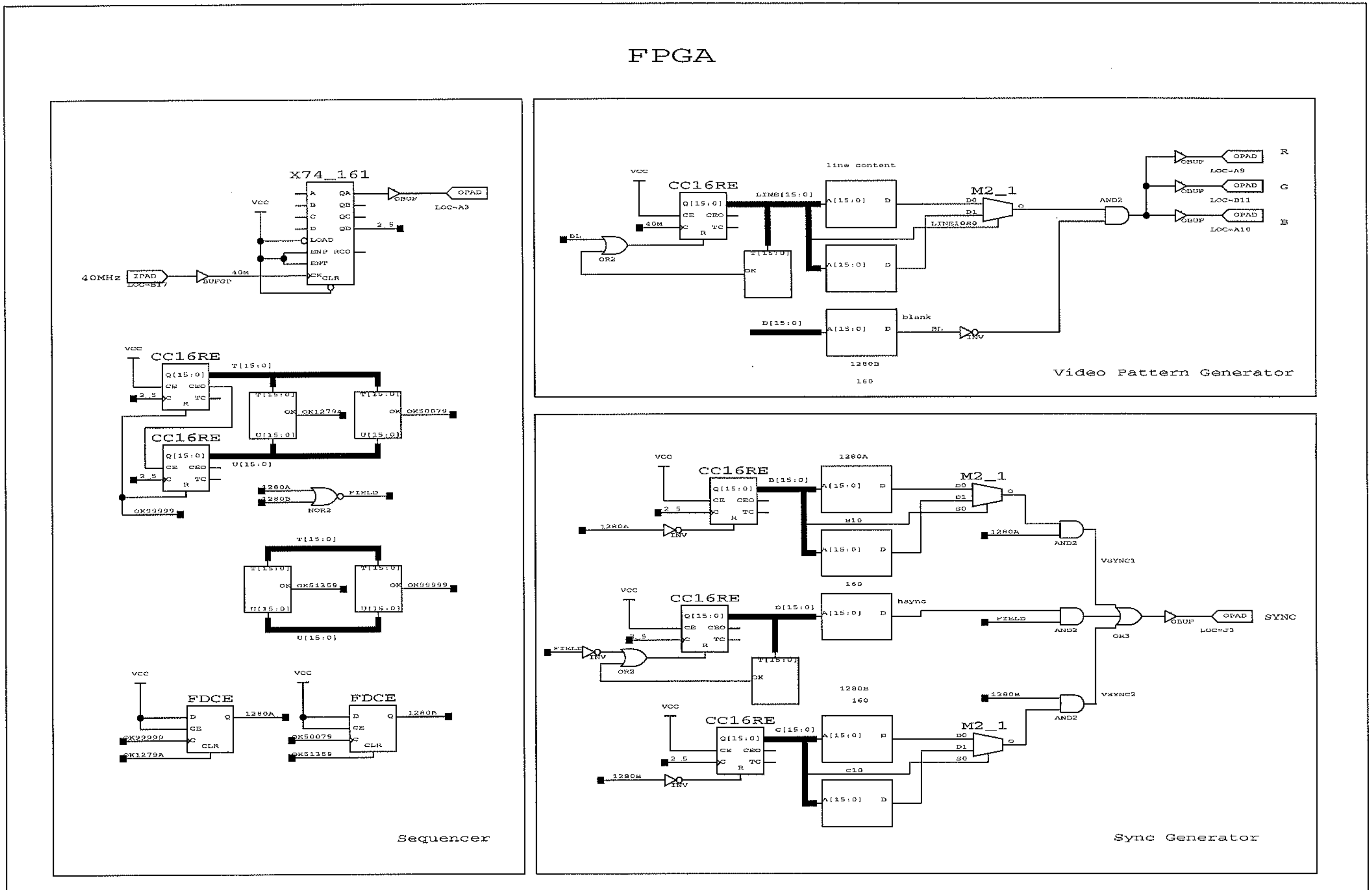

VCC
PULL UP
FPGA
Prom
INIT
DIN
CCLK
PROG
DONE
40MHZ
SYNC
R
G
B
XILINX
XC4013
D 1
CK 2
OE 3
CE 4
XC17256
40 MHz
27.734 MHz
180
180
180
3737737
GND
Video Encoder
CLK
SYNC
R
G
B
N/P
COMP
Y
C
ENC
ASY
AD720JP
to video comp
to Y S-video
to C S-video
VCC
GND
VCC
NTSC
PAL
GND

Fig. 1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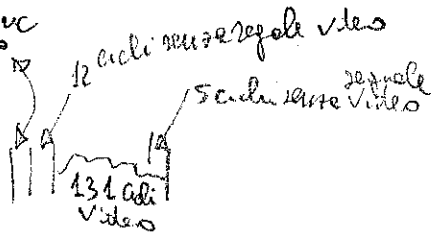
OK50079
OK99999
NOR2
FIELD
1280A
1280B
OK51359
FDCE
OK1279A
Sequencer
line content
LINE[15:0]
LINE1080
M2_1
AND2
R
G
B
LOC=A9
LOC=B11
LOC=A10
OR2
blank
BL
INV
D[15:0]
Video Pattern Generator
B[15:0]
C[15:0]
hsync
VSYNC1
VSYNC2
OR3
LOC=J3
SYNC
Sync Generator

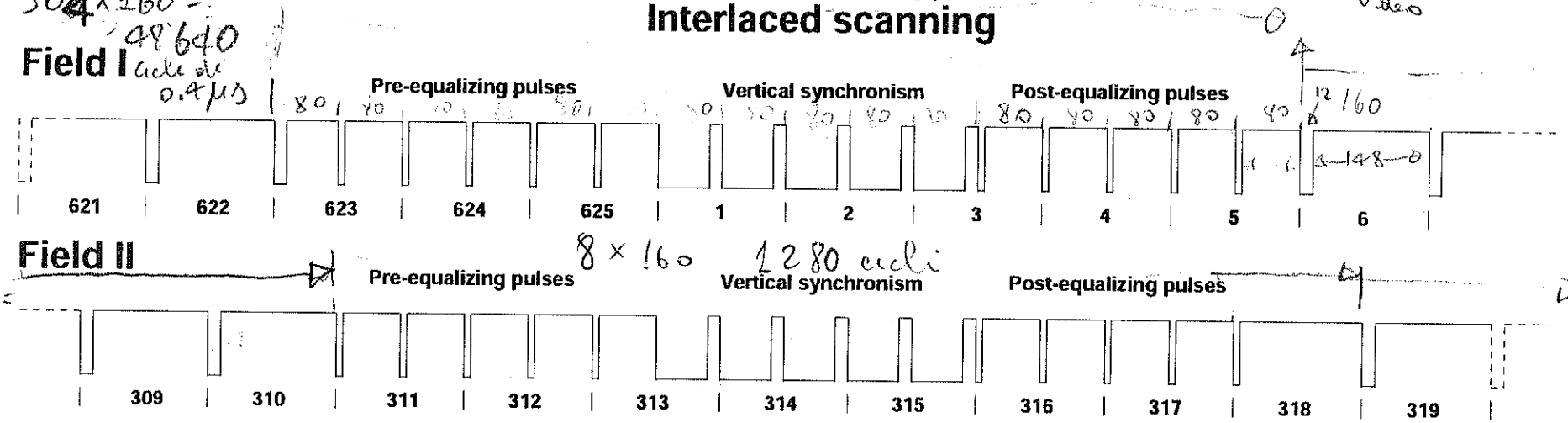
Fig. 2

100'000 cicli di 0.4µs (2.5 MHz)

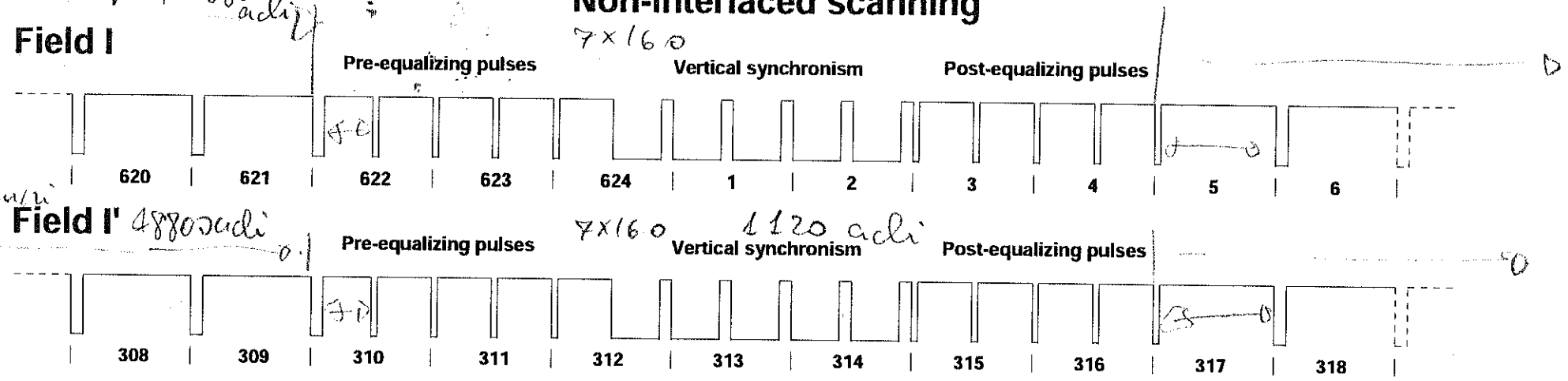
TV scanning methods - PAL-N system



Interlaced scanning



Non-interlaced scanning



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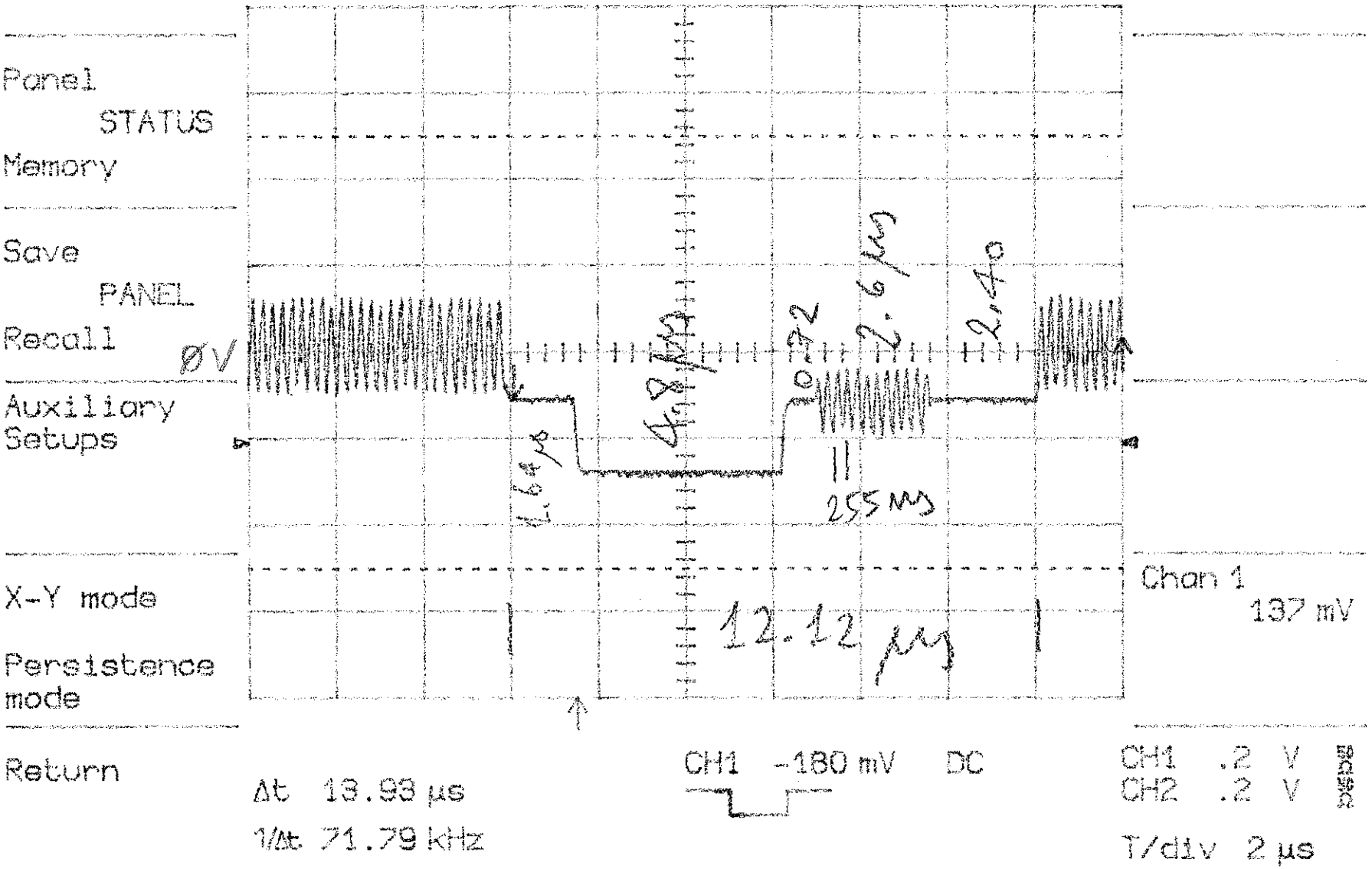

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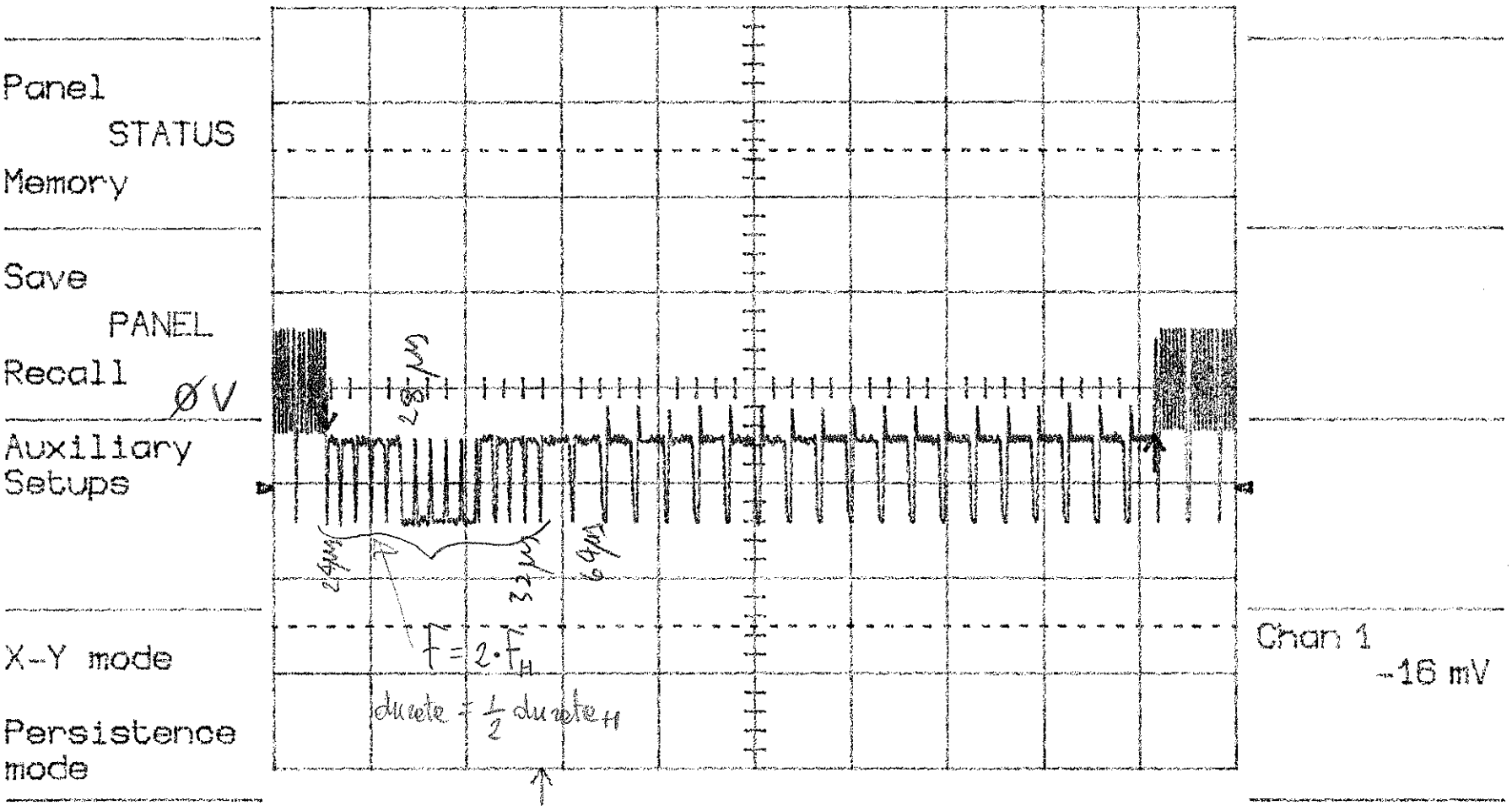

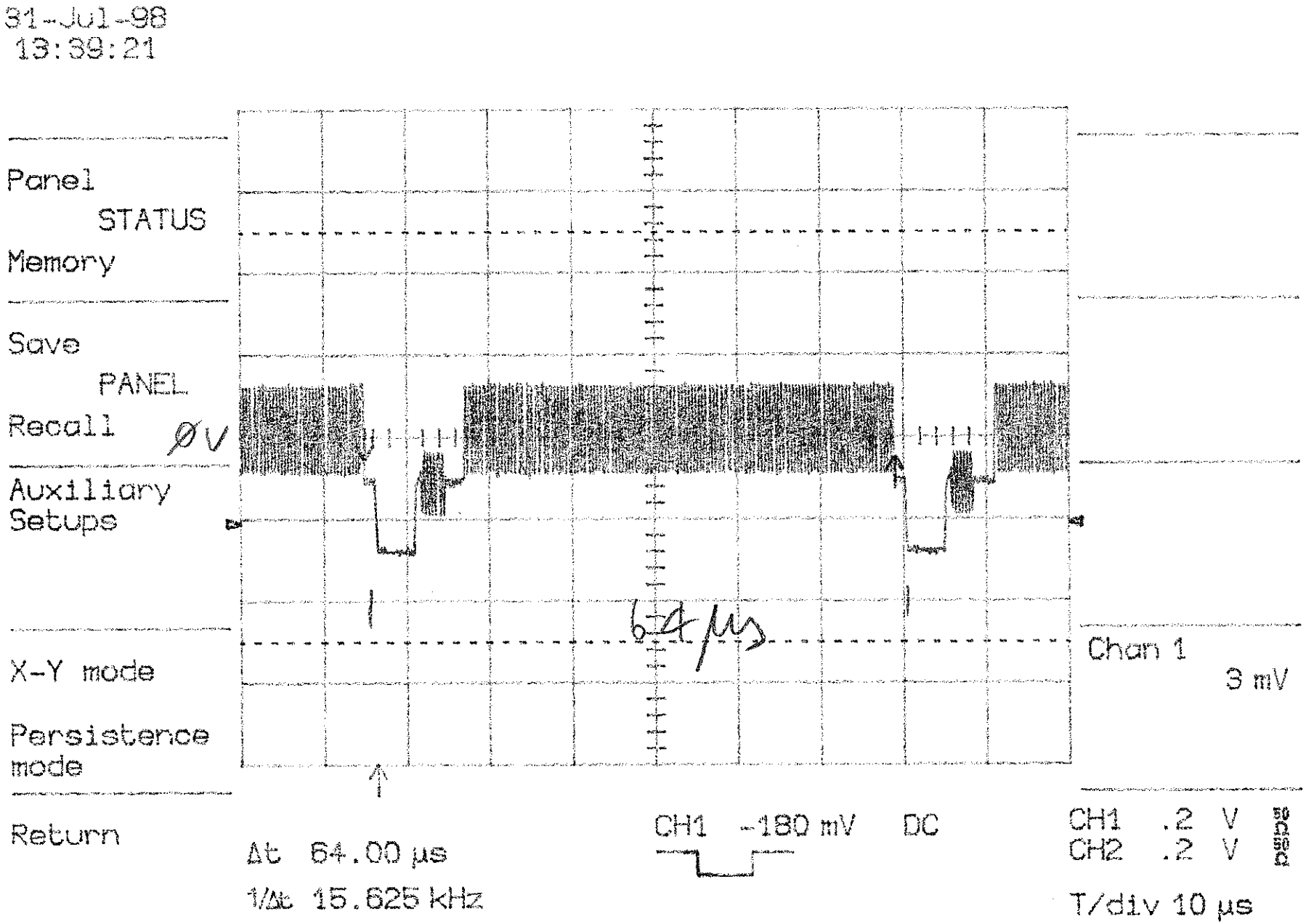
31-Jul-98
13:39:21
Panel
STATUS
Memory
Save
PANEL
Recall
Ø V
Auxiliary
Setups
64 µs
X-Y mode
Persistence
mode
Return
Chan 1
3 mV
Δt 64.00 µs
1/Δt 15.625 kHz
CH1 -180 mV DC
CH1 .2 V
CH2 .2 V
T/div 10 µs