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Studio progettuale di un banco RF per lo studio della risposta di un sistema multifrequenza per la lettura di segnali di matrici di rivelatori per CMB

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IRA 450/11

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1. Introduzione

I Rivelatori ad Induttanza Cinetica (RIC) - in inglese Microwave Kinetic Inductance Detector (MKID) - inizialmente sviluppati dagli scienziati del California Institute of Technology e del Jet Propulsion Laboratory nel 2003, hanno come scopo il rilevamento ad alta sensibilità in campo astronomico di frequenze che vanno dal lontano infrarosso ai raggi X.
Essi sono usati principalmente per la misura del Cosmic Microwave Background (CMB).
Questi dispositivi, che lavorano a temperature criogeniche, tipicamente sotto a 1 grado Kelvin, sono sensori di ultima generazione che si basano sulla presenza di una gap nei livelli energetici del superconduttore. Questo è analogo a quanto accade nei rivelatori a semiconduttore, con la differenza sostanziale che la gap superconduttiva risulta circa mille volte più piccola, permettendo la rivelazione di fotoni di frequenza molto più bassa (da 90 GHz in su).
I fotoni incidenti su una striscia di materiale superconduttivo rompono le coppie di Cooper e creano quasi-particelle in eccesso. L'induttanza cinetica della striscia superconduttiva è inversamente proporzionale alla densità delle coppie di Cooper e di conseguenza l'induttanza cinetica aumenta con l'assorbimento dei fotoni. Questa induttanza è combinata con un condensatore in modo da formare un risonatore a microonde la cui frequenza di risonanza cambia con l'assorbimento dei fotoni. Questo processo di lettura basato su risonatore è utile per sviluppare array con un numero molto elevato di sensori, poiché ogni RIC può essere abbinato ad un singolo tono a microonde e molti sensori possono essere misurati usando un singolo canale a microonde a larga banda, tecnica nota anche come frequency-division multiplexing.

Nello studio preliminare qui presentato, effettuato nel periodo tra Novembre 2008 e Febbraio 2009, è stato preso in esame il progetto del sistema a radiofrequenza di generazione, modulazione, demodulazione e rivelazione dei segnali di eccitazione di un array di sensori MKID.
In particolare sono state considerate due diverse soluzioni: una soluzione con sistema di processing in banda base di tipo digitale e una soluzione con sistema di processing in banda base di tipo analogica.
La differenza fra le due soluzioni esaminate risiede nel sistema di acquisizione e processamento dei segnali in uscita dal blocco MKID già convertiti in banda base, mentre entrambe si basano sullo stesso sistema di generazione, modulazione e demodulazione dei segnali di eccitazione del blocco MKID.
E' importante sottolineare che questi due approcci, molto diversi fra loro, non sono l'uno in

alternativa all'altro, bensì rappresentano due passaggi strettamente legati alla fase di sviluppo del progetto in questione.

Per chiarire quanto detto si faccia riferimento, per il momento, alle figg. 1 e 2.

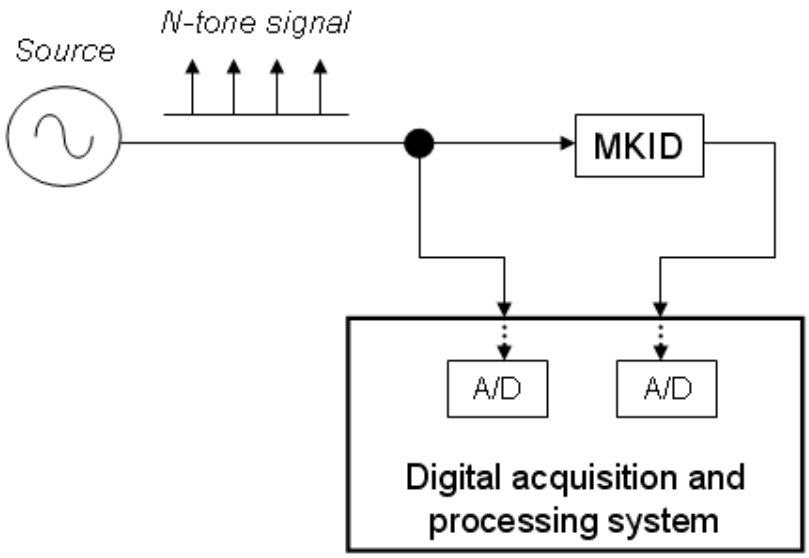


Fig. 1: sistema di processing digitale.

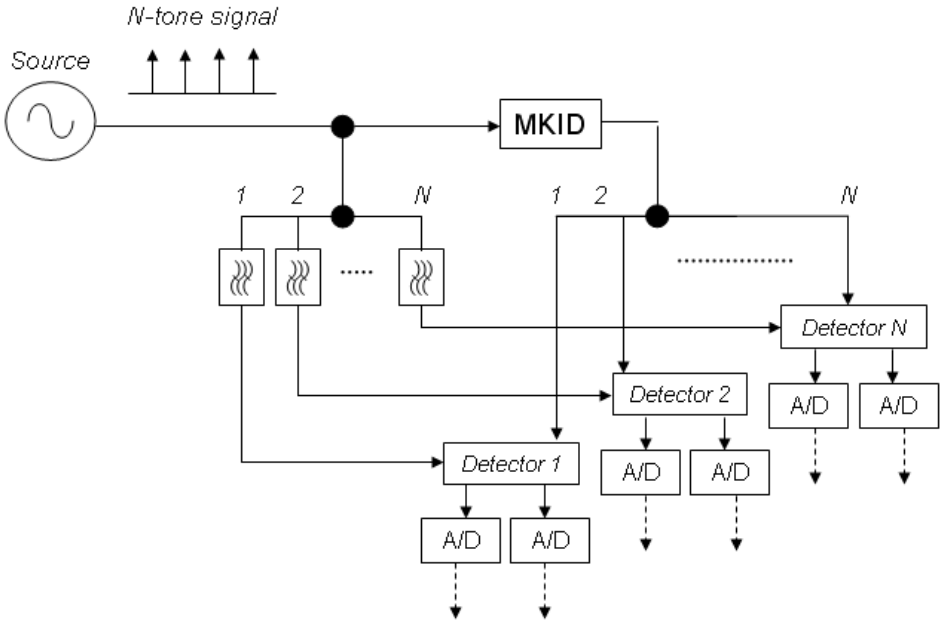


Fig. 2: sistema di processing analogico.

In fig. 1 è presentato lo schema molto semplificato del sistema digitale, mentre in fig. 2 l'equivalente sistema analogico.

Senza entrare ancora nei dettagli, nel primo caso le operazioni per la misura della differenza di fase e ampiezza fra il segnale di ingresso e quello di uscita dal blocco MKID vengono svolte da un

sistema digitale ad elevata sampling rate ed elaborazione dati; in prima approssimazione con solo due convertitori analogico-digitali (A/D) è possibile gestire la misura su un certo numero di sensori KID contemporaneamente.

Nel secondo caso invece sono necessari tanti rivelatori quanti sono i sensori KID da misurare: i rivelatori forniscono in uscita due segnali, uno proporzionale alla differenza di fase e l'altro a quella di ampiezza. Questi due segnali vengono poi campionati dai corrispondenti convertitori A/D: ogni rivelatore necessita quindi di due A/D.

L'approccio di tipo analogico è sicuramente più semplice e più veloce e meno costoso da realizzare se si vuole effettuare la misura su un numero molto ristretto di sensori KID (es. 8).

Al contrario, nel caso si voglia estendere la misura su un numero molto elevato di sensori, questo sistema diventerebbe estremamente complesso tanto da non essere assolutamente gestibile; sarebbe quindi quasi obbligato il passaggio ad un sistema digitale, sicuramente complesso da programmare ma che costituirebbe l'unica soluzione per gestire una matrice molto grande di sensori (è da valutare qual è il limite superiore).

Riassumendo, nella prima fase del progetto, cioè quando si hanno pochi sensori KID da misurare parallelamente (in questo caso 8), è indispensabile la realizzazione di un sistema analogico; questo soprattutto per tre motivi:

1) si affronta il progetto ad un livello più basso di complessità permettendo di maturare esperienza sulle problematiche realizzative legate a questo tipo di applicazione;
2) il gruppo scientifico può disporre di un primo banco di test, composto da un numero ristretto di sensori, utilizzabile in tempi ragionevoli;
3) il sistema analogico diventa il sistema di riferimento per una eventuale estensione del progetto, finalizzata alla lettura di una matrice molto grande di sensori (approccio di tipo digitale).

La relazione dell'attività in oggetto sarà così strutturata: inizialmente verrà presentata una breve descrizione di entrambe le architetture proposte, la trattazione avrà carattere del tutto generale con l'illustrazione degli schemi a blocchi.

Successivamente si passerà ad un'analisi più accurata che, partendo dalle specifiche di progetto, mostrerà i risultati di alcune simulazioni per determinare le configurazioni migliori delle catene di modulazione, demodulazione e rivelazione.

Le soluzioni più interessanti e degne di ulteriore approfondimento saranno elencate in una tabella riassuntiva.

2. Sistema di generazione, modulazione e demodulazione dei segnali di eccitazione

Questa, come detto, è la parte comune alle due soluzioni.

Di seguito viene riportata (come esempio) l'architettura del sistema digitale (fig. 3) da considerarsi solamente come riferimento alla descrizione qui presentata.

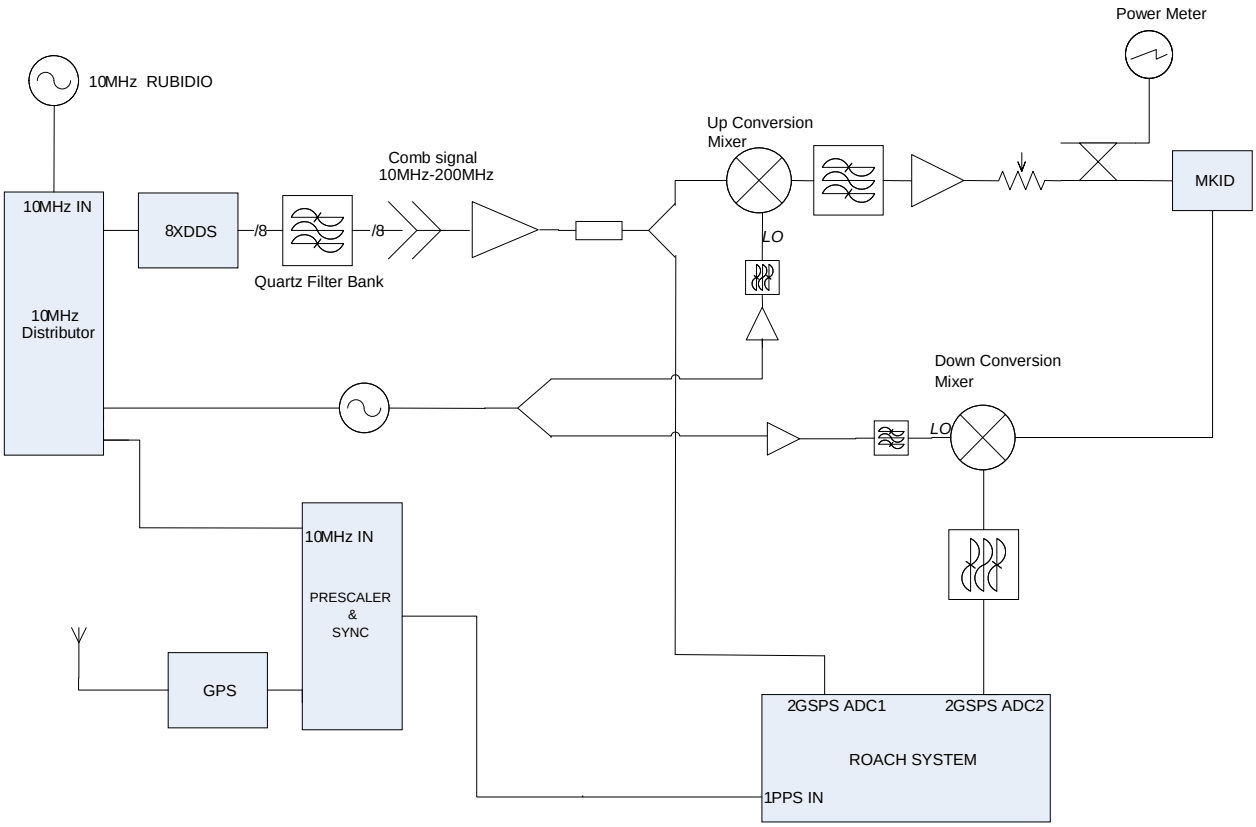


Fig. 3: architettura del sistema digitale.

Otto segnali monocromatici, separati fra loro di circa 10 MHz in frequenza, vengono parallelamente generati da un blocco 8xDDS (*Digital Direct Synthetizer*) programmato che può lavorare fino a 400 MHz. Il datasheet del dispositivo DDS è riportato come allegato in fondo al documento.

Questi otto segnali entrano in un banco di filtri molto selettivo (Quartz Filter Bank).

Quest'ultimo serve per eliminare spurie e armoniche generati dal blocco 8xDDS: armoniche e prodotti spuri potrebbero ingenerare intermodulazioni non desiderate.

Gli otto segnali in uscita dal banco di filtri vengono sommati fra loro (Signal Combiner 10MHz-200MHz) in modo da formare un pettine in frequenza (fig. 4), amplificati e successivamente convertiti in alta frequenza (Up-Conversion), in particolare alla frequenza di risonanza dei sensori

KID, grazie ad una portante generata da un sintetizzatore.

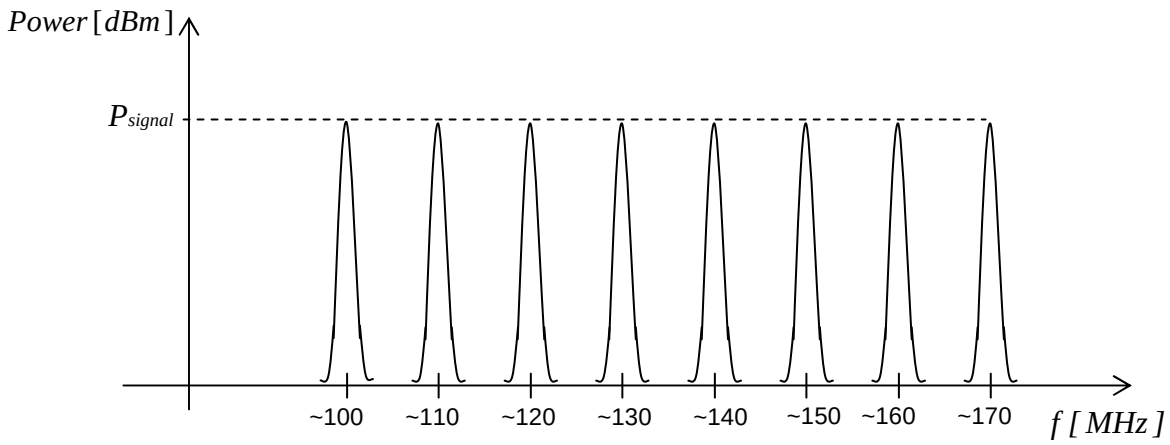


Fig. 4: pettine (in frequenza) di segnali in uscita dal Signal Combiner 10MHz-200MHz.

Si precisa che in questo progetto i segnali convertiti in alta frequenza potranno coprire due bande di frequenze: 2,9-3,2 GHz e 4,1-4,9 GHz.

Un filtro passa banda dopo l'Up-Conversion è necessario per eliminare i prodotti multipli generati dal mixer.

Un'eventuale amplificazione dei segnali deve essere calcolata opportunamente in base al livello necessario per l'eccitazione dei sensori (si veda "Calcolo del guadagno e del noise di catena").

L'Accoppiatore Direzionale e il Power Meter servono per monitorare il segnale all'ingresso del blocco MKID.

La Down-Conversion, sincrona alla stessa frequenza (Oscillatore Locale) usata in Up-Conversion riporta in banda base i segnali all'uscita di MKID.

Il filtro passa banda all'uscita del mixer è necessario per eliminare i prodotti multipli generati dal dispositivo stesso.

Sul ramo dell'Oscillatore Locale (*LO, Local Oscillator*) dei due Mixers (Up e Down Conversion) sono necessari amplificatori e filtri per portare il livello di segnale del sintetizzatore al valore di pilotaggio necessario per il funzionamento corretto dei Mixers stessi (almeno +4 dBm).

Il datasheet del mixer di Up Conversion (e Down Conversion) è riportato come allegato in fondo al documento.

Il componente 8xDDS, il generatore dell'Oscillatore Locale dei Mixers e il sistema di acquisizione in banda base sono tutti sincronizzati dal segnale a 10 MHz prodotto da un generatore al rubidio. Questo segnale di sincronismo viene equamente distribuito ai circuiti sopracitati da un sistema ad alto isolamento fra le porte (10 MHz Distributor).

L'acquisizione è sincronizzata da un segnale PPS (*Pulse Per Second*) generato da un Prescaler che

divide il segnale di riferimento a 10MHz.
Tale segnale è a sua volta sincronizzato da un segnale generato dal riferimento secondario che potrebbe essere un modulo GPS. In questo modo si garantisce la coerenza dei segnali acquisiti dagli ADC (*Analog to Digital Converter*). Il GPS può fornire gli "stamps" temporali collezionati dal computer *host* che servono ad etichettare i dati acquisiti.

3. Architettura del sistema digitale

Si faccia riferimento ancora una volta allo schema di fig. 3.
All'uscita del blocco MKID il segnale viene demodulato /filtrato in banda base (fino a 400MHz) e campionato direttamente dagli ADC2 del sistema Roach alla frequenza di almeno 1 GSample/sec.
Sull'altro canale (ADC1) il sistema Roach acquisisce il segnale di eccitazione (fino a 400 MHz), somma degli 8 DDS, sempre alla frequenza di 1 GSample/sec.
Questo segnale infatti viene diviso da un Power Splitter x2 prima di entrare nel mixer di UpConversion.
Sul firmware della scheda Roach verrà caricato un progetto in grado di eseguire le operazioni necessarie per misurare la differenza di fase/ampiezza fra il segnale all'uscita di MKID e il segnale somma.
Il sistema Roach ha bisogno in ingresso di un segnale che generi il clock digitale per il sistema di acquisizione. E' da stabilire se questo segnale può essere fornito dal generatore dell'Oscillatore Locale dei due mixers; in questo caso questo segnale deve essere opportunamente diviso in frequenza da un Prescaler e poi squadrato da uno Square Generator.
In caso contrario bisogna utilizzare un altro sintetizzatore, il cui segnale deve essere squadrato anche in questo caso.

Pregi:

- Il sistema digitale è modulare: in linea teorica con solo 2 ADC si possono controllare un grosso numero di sensori KID; questo numero, che deve essere ancora valutato, dipende dalla capacità dei moduli FPGA (*Field Programmable Gate Array*) della scheda Roach e da quanto pesante diventa il firmware in essa installato.
  Per misurare matrici di sensori più grandi si possono comunque parallelizzare più Roach systems, utilizzando lo stesso firmware e mantenendo in generale la stessa architettura

sopra descritta.

Difetti:

- Il sistema Roach richiede man power dedicata per la sua programmazione.

Oltre ai pregi e ai difetti di questo sistema, va tenuto presente anche un aspetto di primaria importanza legato alle schede A/D ad elevata velocità. Queste schede generalmente hanno un numero limitato di bit (es. 8) per la quantizzazione del segnale. Bisogna valutare se il minore numero di bit può essere compensato dall'elevata sampling rate e velocità di elaborazione, in rapporto alla dinamica richiesta da questo tipo di applicazione.

4. Architettura del sistema analogico

In questo caso è necessario riferirsi allo schema di fig. 5.

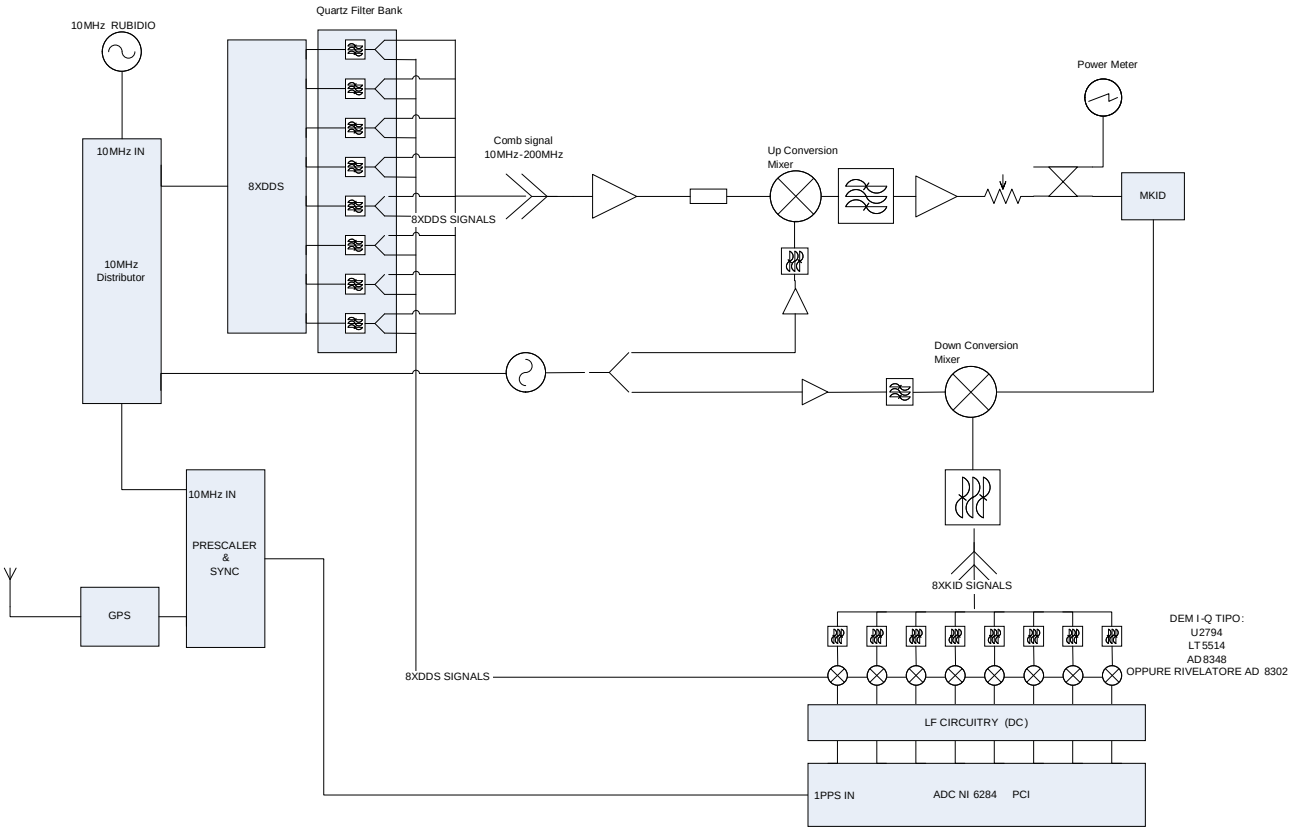


Fig. 5: architettura del sistema analogico.

Ciascun segnale generato dal blocco 8xDDS, una volta pulito da eventuali armoniche e spurie

mediante il rispettivo filtro del banco (Quartz Filter Bank), deve essere diviso da un Power Splitter X2 in modo da effettuare la rivelazione della differenza di fase e ampiezza su ogni singolo segnale in uscita dal blocco MKID (rispetto a quello di ingresso), già portato in banda base e filtrato.
Gli otto segnali in uscita dal Quartz Filter Bank vengono comunque sommati fra loro, prima della UpConversion, per generare il singolo segnale di eccitazione fino a 400MHz (pettine).
Per isolare ogni singola risposta del MKID ed evitare che i prodotti di intermodulazione generino risposte spurie, ogni risposta di ogni singolo KID deve essere filtrata con un filtro passa banda opportunamente sintonizzato alla corrispondente frequenza di risonanza prima della fase di rivelazione.
L'acquisizione di ogni segnale in uscita dai rivelatori (sono praticamente componenti continue) può essere fatta da sistemi in multiplexing come quello della National Instrument (massimo 32 canali→16 KID). Il datasheet di questa scheda di acquisizione è riportato come allegato in fondo al documento.
Prima di entrare nei convertitori A/D, i segnali in uscita dai rivelatori potrebbero dover essere ulteriormente amplificati e filtrati a seconda della dinamica degli A/D stessi (LF cicuitry (DC)).

Pregi:

- Le operazioni per la rivelazione possono essere fatte da sistemi analogici molto semplici (vedi Datasheet allegati) e poco costosi;
- Il sistema è poco complesso e facile da testare.

Difetti:

- Aumento del cablaggio a causa della distribuzione di ogni singolo segnale generato dal DDS per la rivelazione.
- Sistema poco modulare: l'acquisizione di un alto numero di sensori dipende dal controllo di diversi ADC in multiplexing.
- Problema di stabilità del guadagno e dell'offset nell' amplificazione in DC dei segnali dei KIDs demodulati. In generale questo problema viene riscontrato negli amplificatori in DC a causa della dipendenza dalla temperatura dei parametri dei componenti elettronici. Inoltre sono soggetti al rumore 1/f, che può essere molto superiore al rumore di origine termica (Johnson). Gli effetti di questo fenomeno indesiderato sono da valutare ed eventualmente da controbattere.

5. Calcolo del guadagno e del noise della catena di modulazione

Prima dell'inizio dell'attività sono state fornite le principali specifiche di progetto in termini di livello di segnale (S) e di rapporto segnale rumore (S/N), come rappresentato in fig. 6:

- livello di segnale all'ingresso del blocco MKID (fuori dal criostato): -20÷-30 dBm circa;
- livello di segnale all'ingresso dei sensori KID (stadio a 300mK): -50÷-60 dBm circa;
- livello di S/N all'ingresso dei sensori KID (stadio a 300mK): 60 dB circa;

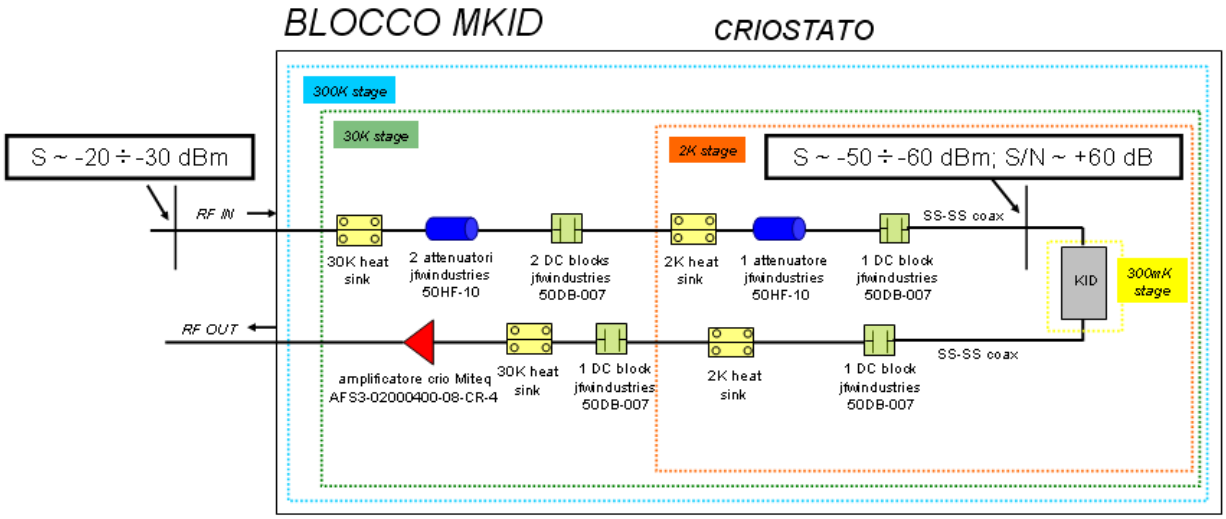


Fig. 6: schema a blocchi del sottosistema MKID con le relative specifiche di progetto.

Partendo da queste specifiche, attraverso opportuni calcoli del rumore generato da apparati rumorosi in cascata a temperature diverse come è il caso in esame, si è determinato il rapporto segnale rumore minimo all'ingresso del blocco MKID: esso è stato stimato essere pari a circa 61 dB.

Per rispettare questa specifica, partendo dalle caratteristiche di phase noise del dispositivo 8XDDS (vedi datasheet allegato) e considerando una banda istantanea di 100 KHz su ciascun canale (determinata dalla banda passante dei filtri al quarzo), si è calcolato il massimo valore di NF (*Noise Figure*), generato dalla catena di modulazione, che può essere accettato all'ingresso del blocco MKID. Questo valore è circa pari a 9 dB.

A questo punto si è passati alla simulazione del guadagno complessivo e della NF di catena per trovare la migliore configurazione dello schema a blocchi del sistema di modulazione, già descritto precedentemente in linea generale.

La soluzione che è sembrata essere quella ottimale, in grado di soddisfare le specifiche richieste, è quella rappresentata in fig. 7.

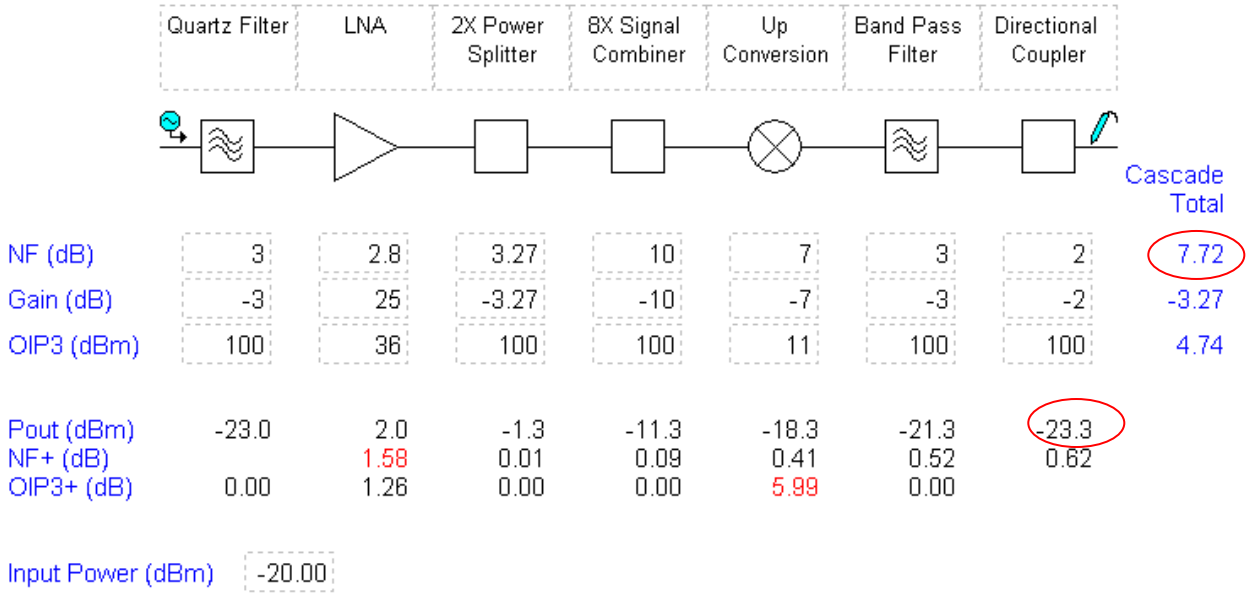


Fig. 7: simulazione del guadagno e della NF della catena di modulazione.

Contrariamente a quanto asserito prima, è presente un unico stadio di amplificazione e questo viene inserito subito a valle del filtro al quarzo, affinché venga rispettata la specifica sulla NF.

Questo significa che è necessario un LNA (*Low Noise Amplifier*) per ogni segnale generato dal DDS (cioè 8).

La simulazione è stata effettuata ipotizzando una potenza del segnale di ingresso pari a -20 dBm (generata dal DDS) e impostando i valori di GAIN, NF e OIP3 (*Output Intercept Point of 3rd order*) del LNA con quelli di un amplificatore monolitico a basso rumore trovato commercialmente.

6. Studio preliminare dello schema a blocchi della catena di demodulazione e rivelazione nel sistema analogico

Dopo aver preso in esame la catena di modulazione, si è passati allo studio della catena di demodulazione (e successiva rivelazione) del sistema analogico.

Da una prima indagine commerciale sono stati individuati alcuni dispositivi adatti alla funzione di rivelazione della differenza di fase/ampiezza fra il segnale di uscita dal blocco MKID ed il segnale di ingresso. Si tratta di demodulatori I-Q (es. U2794B Atmel, AD8348 Analog Devices) oppure di RF/IF Gain and Phase Detector (es. AD8302 Analog Devices). Si vedano a tal proposito i data sheet allegati.

Questi circuiti possono funzionare indicativamente con segnali di ingresso aventi:

- P_{INmin} = ~ -60 dBm;
- P_{INopt} = ~ -30 dBm;
- P_{INmax} = ~ -10 dBm.

Considerando le specifiche sopra riportate e che il livello del segnale, dalla sezione di ingresso dei sensori KID all'uscita del criostato, guadagna complessivamente circa 15 dB (vedi fig. 8), si sono impostate alcune simulazioni per trovare, anche in questo caso, la migliore configurazione dello schema a blocchi del sistema di demodulazione e rivelazione.

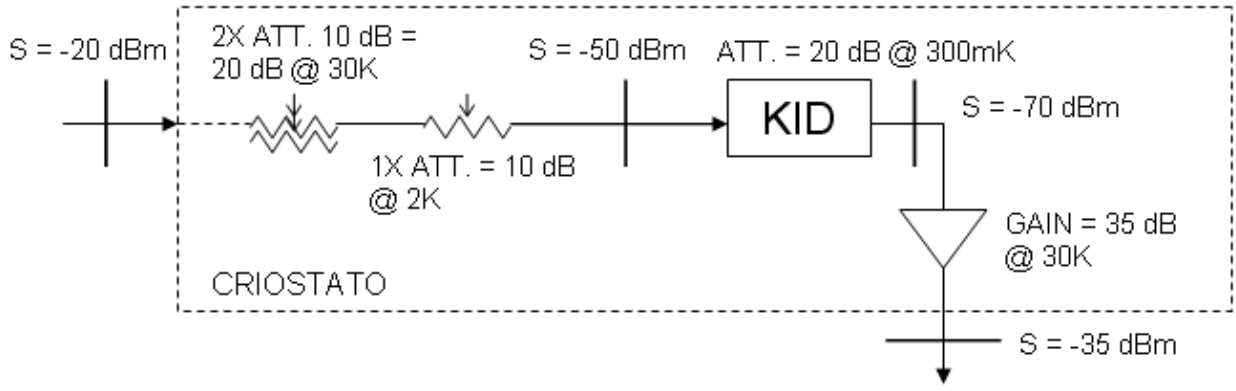


Fig. 8: livello del segnale dalla sezione di ingresso dei sensori KID all'uscita del criostato.

Per quanto riguarda lo schema della catena di demodulazione, mantenendo nella catena di modulazione gli stessi componenti elettronici ipotizzati nella precedente simulazione (vedi fig. 7), quindi Input Power pari a -39 dBm, secondo quanto detto precedentemente, la soluzione che è sembrata più promettente è stata quella di fig. 9.

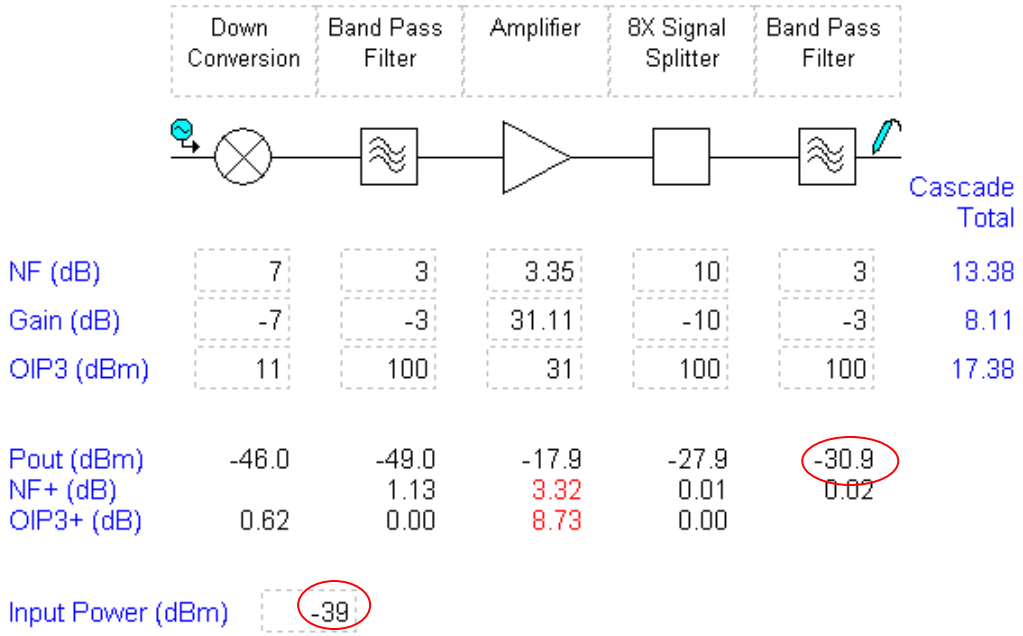


Fig. 9: simulazione della catena di demodulazione.

Inserendo nella catena di demodulazione un amplificatore monolitico ad elevato guadagno e bassa NF (si trova in commercio già connettorizzato) si ottiene una Output Power di circa -31 dBm come da specifica.

A questo punto è necessario verificare il livello degli otto segnali (uguale per tutti e 8) sulla sezione del secondo ingresso dei dispositivi di rivelazione (in fig. 10 viene evidenziata la numerazione degli ingressi dei dispositivi di rivelazione).

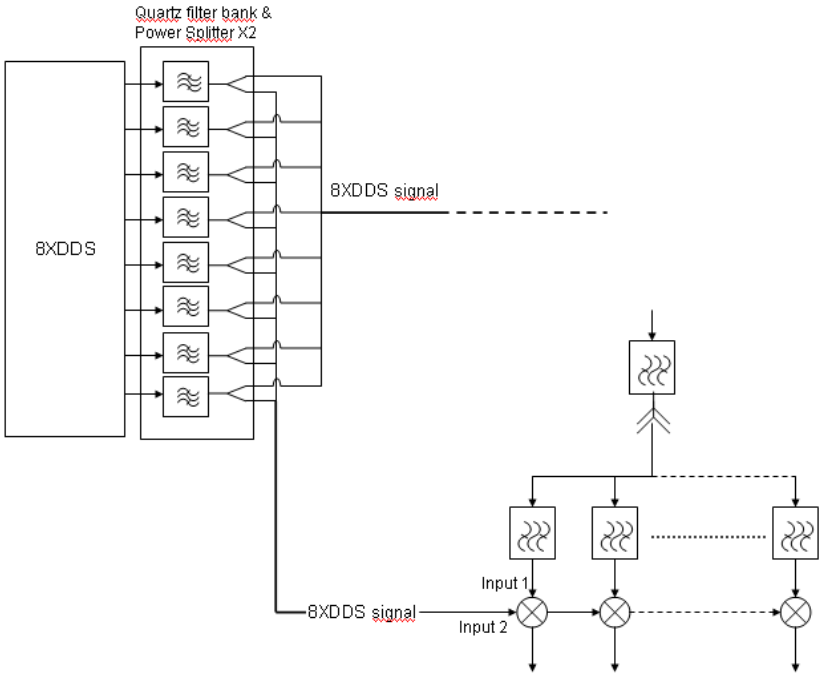


Fig. 10: numerazione degli ingressi dei dispositivi di rivelazione

Dalla simulazione si è trovato il seguente risultato (fig. 11).

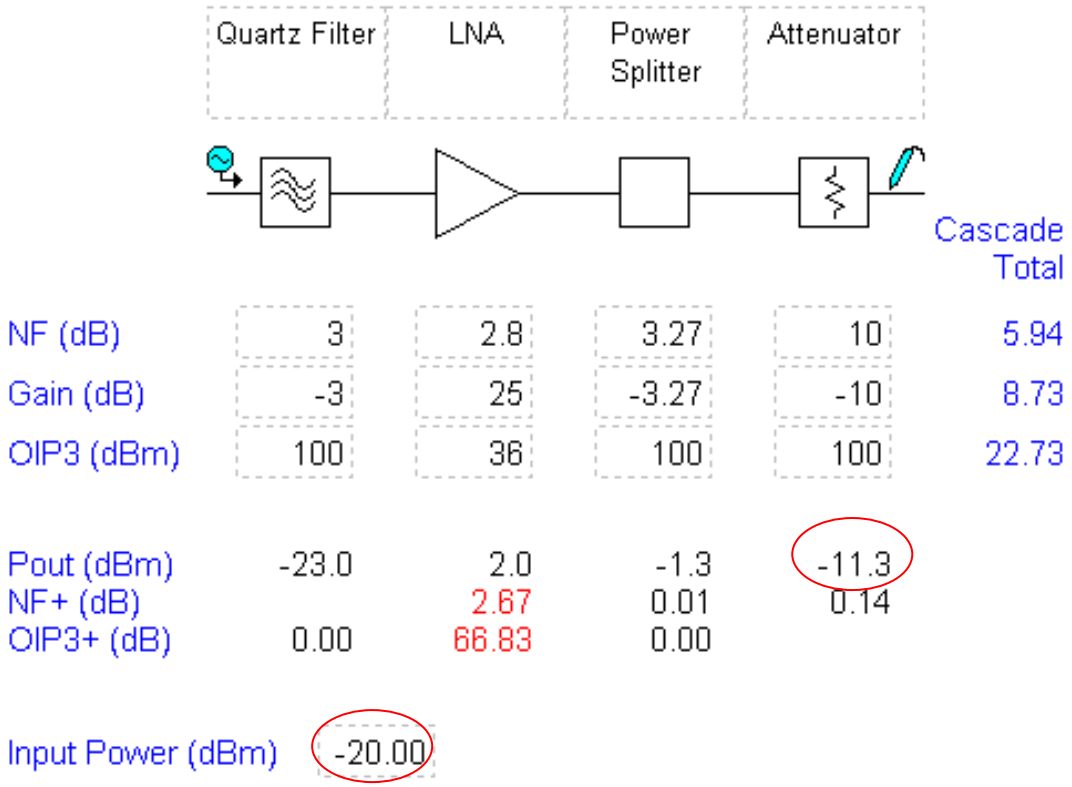


Fig. 11: simulazione del livello dei segnali sulla sezione del secondo ingresso dei dispositivi di rivelazione.

Anche in questo caso la simulazione è stata effettuata facendo riferimento alla catena di modulazione di fig. 7 (in particolare stesso LNA e stessa Input Power).

Come si può notare dallo schema a blocchi, si è dovuto inserire un blocco di attenuazione a valle del Power Splitter per ottenere una Output Power inferiore a -10 dBm.

Dovrà essere valutato se sarà necessario aggiungere ulteriori blocchi di attenuazione in questa catena per migliorare le prestazioni dei dispositivi di rivelazione (portare il livello del segnale su *input 2* a ~ -30 dBm).

Un'altra soluzione interessante che si potrebbe adottare è quella di eliminare un blocco di attenuazione (10 dB) all'interno del criostato a 30K in modo che, mantenendo l'architettura già discussa (simulazioni precedenti) e abbassando a ~ -30 dBm la potenza fornita dal blocco 8XDDS, è possibile rimanere entro le specifiche senza aggiungere (comunque da verificare) alcun blocco di attenuazione nella catena del secondo ingresso del rivelatore.

Si precisa che quanto detto sopra è giustificato dal fatto che l'eliminazione di un blocco di attenuazione (10 dB) nello stadio a 30 K del criostato non modifica sostanzialmente la specifica su NF all'ingresso del blocco MKID.

Qui di seguito una tabella riassuntiva con le soluzioni migliori fin qui trovate.

P_{DDS} (dBm)	NF (dB)	P_{inMKID} (dBm)	$P_{outMKID}$ (dBm)	$P_{in1DETECT}$ (dBm)	$P_{in2DETECT}$ (dBm)	ATT. 10 dB Input2 Detector	ATT.10dB @ 30k
-20	7.8	-24	-39	-31	-10	SI	SI
-30	**7.8**	**-34**	**-39**	**-31**	**-10**	**NO**	**NO**

La seconda soluzione è stata evidenziata in quanto ottimizzata rispetto alla precedente.
Prima di concludere questo paragrafo è necessario fare alcune considerazioni.
Dato che alcuni dei rivelatori trovati sul mercato offrono le migliori prestazioni quando i segnali di ingresso sono in quadratura (sfasati di 90°), si sono ripetute le simulazioni sostituendo lo splitter X2 con un ibrido a 90°. I risultati ottenuti (fig. 12) non si discostano quasi per niente con quelli già discussi precedentemente.

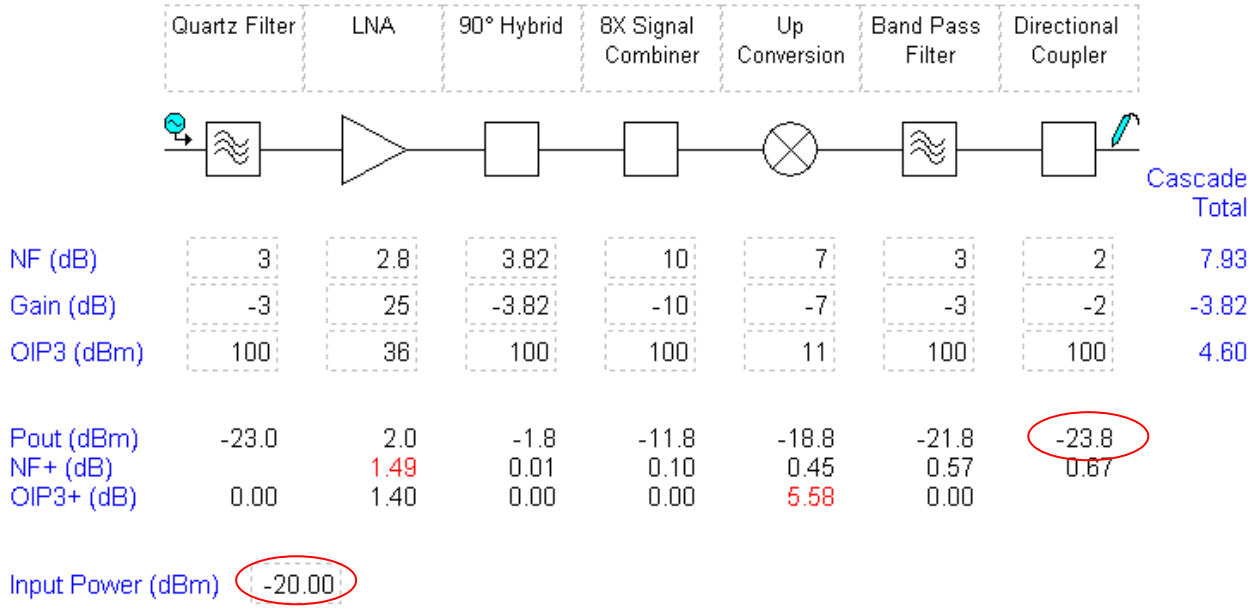


Fig. 12: simulazione del guadagno e della NF della catena di modulazione sostituendo lo splitter X2 con un ibrido a 90°.

Inoltre all'uscita di ciascun rivelatore, prima di entrare nell'ADC, potrebbe essere necessario inserire uno stadio di amplificazione, seguito da un filtro passa basso, per garantire un livello sufficientemente alto del segnale che assicuri il corretto funzionamento del convertitore analogico-digitale. Questo sarà da valutare una volta che verrà testato il reale livello di segnale in uscita dai rivelatori e tenendo in considerazione la dinamica dell'A/D.

Si allega qui di seguito (fig. 13) un possibile schema del blocco amplificatore e filtro passa basso.

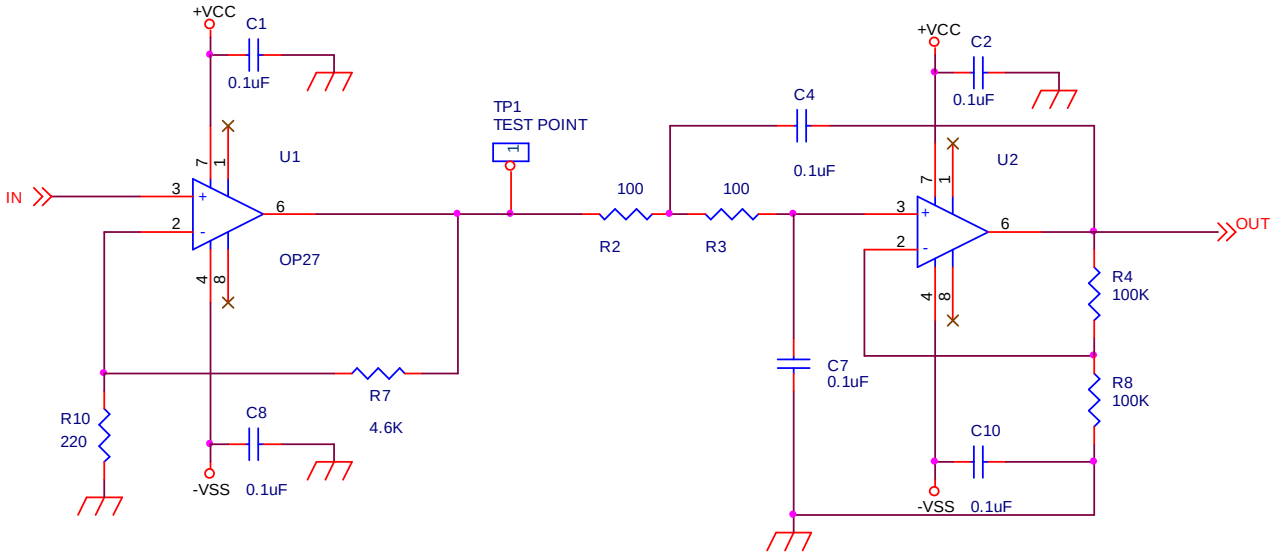


Fig. 13: possibile schema del blocco amplificatore e filtro passa basso.

Di seguito si riportano in allegato i datasheet di alcuni componenti selezionati per il progetto.

INSTRUMENTS, INC.

4 Channel 400MHz DDS Signal Generator

Model 1940A

The Model 1940A is a four channel 400MHz DDS Signal Generator in a rackmount (1U) instrument case. The 1940A generates up to four different output frequencies simultaneously from 200kHz to 400MHz in 1Hz steps. The 1940A can be locked to an external frequency standard or used stand-alone with its internal temperature compensated crystal oscillator (TCXO). Sine waves with up to 60dB of attenuation are standard. The 1940A can be configured with 2 or 4 (standard) frequencies. Simple front panel control or RS232 allows setting of all parameters, which can be saved into non-volatile EEPROM memory upon power down. The 1940A is an ideal high frequency upgrade for the 2910B/RACK.

Specifications:

OUTPUT

TYPES: Sinewave.
IMPEDANCE: 50Ω, Sine.
RANGE: 200kHz to 400MHz in 1Hz steps.

AMPLITUDE

Sine: approx. +4dBm ($1V_{pp}$ at 25MHz) into 50Ω. Front panel or RS232 programmable step attenuator from 0 to 60dB on two channels in each group. ±6dB, 1MHz to 400MHz at 0dB attenuation.

CONTROL

Three front panel buttons and a rotary encoder per section allow setting of frequency and menu selections. The same functions can be set using RS232 to 19.2kBaud. Output Frequency, status and menus are displayed on a 2-line LCD for each section. Other than AC line power, each synthesizer section is independent.

ACCURACY AND STABILITY (internal clock)

On-board TCXO gives <±1.5ppm at 18-28 ^{o}C. The internal TCXO is stable to an additional ±2ppm per year, 18-28 ^{o}C.

LOCK TO EXTERNAL STANDARD

LEVEL: 0.5-3Vrms Sine or Square Wave can be applied to the EXT STD Input BNC. 50Ω.
EXT. STD. FREQUENCY: 1, 2, 5, 10, 1.544 (T1), or 2.048MHz (E1), selectable from front panel or serial commands. When locked, the accuracy and stability of the 1940A are equal to those of the standard.
LOCK RANGE: The 1940A will lock and track an EXT. STD. input as long as the frequency is equal to the selected frequency ±5ppm (typically ±10ppm).

SPECTRAL PURITY (sine output, 50Ω load)

Phase Noise: <-120dBc, 10kHz offset, 10MHz out.

Spurious:
<-50dBc below 10MHz (typ. 500MHz span)
<-45dBc below 80MHz
<-40dBc below 160MHz
<-35dBc below 400MHz

Harmonic:
<-50dBc below 1MHz
<-45dBc below 20MHz
<-40dBc below 80MHz
<-35dBc below 160MHz
<-30dBc below 400MHz

Output-output isolation >40dBc.

POWER REQUIREMENTS

120/240VAC, 50VA Max. 50/60Hz.

ENVIRONMENTAL

Temperature: +5^{o}C to +40^{o}C operating.
Humidity: 80% to 31^{o}C, decreasing to 50% at 40^{o}C.

STANDARD CONFIGURATIONS

1940A/S-04: eight Sine Outputs, BNC connectors, four frequencies, four attenuators, two displays.

Consult factory for other configurations.

11-Apr-2006

NOVATECH INSTRUMENTS, INC.
P.O. Box 55997
Seattle, WA 98155-0997
United States of America
http://www.novatech-instr.com/
sales@novatech-instr.com
206.363.4367 FAX/206.301.8986 Voice

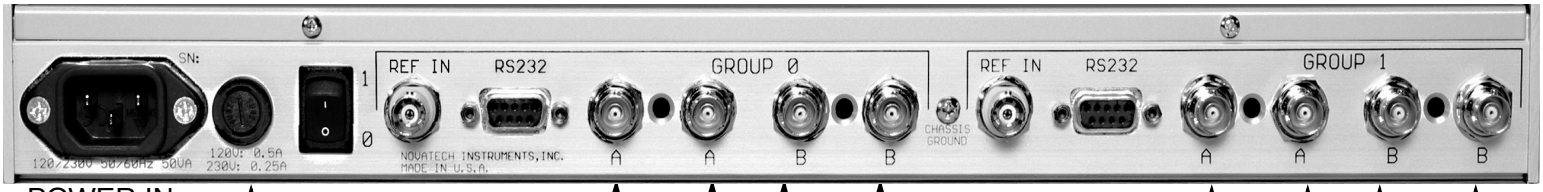
Table 1: 2910A Legacy Serial Commands

RS232 Command	Function
F XXX.XXXXXX	Set Frequency in MHz to nearest 1Hz. Decimal point required. Both outputs set to same frequency. Maximum frequency 399.999999MHz.
E x	x=D for Echo **D**isable, x=E for Echo **E**nable
P x	x=D, power up with default settings; x=S, power up with Saved Settings
Reset	This command resets the 1940A. EEPROM data is preserved and, if valid, is used upon restart. This is the same as cycling power.
Reset All	This command clears the EEPROM valid flag and restores all factory default values.
X n	n=D, 1, 2, 3, 4, 5, or 6. Use to select a preset reference value. Setting n=D selects the internal clock. If n=1, selects 5MHz external reference; n=2, selects 10MHz. Values 3, 4, 5 and 6 have been added to the 1940A. Setting a 3 selects 1MHz, 4 selects 2MHz, 5 selects 1.544MHz and 6 selects 2.048MHz.

Table 2: 1940A Serial Commands

RS232 Command	Function
Fx XXX.XXXXXX	Set Frequency in MHz to nearest 1Hz. Decimal point required. x=a or b, depending upon which frequency is set. In a 4-frequency system, there are two serial ports, each requiring Fa and Fb. Maximum frequency 399.999999MHz.
Qe	Query the non-volatile memory (EEPROM) storage. See manual for details of returned information.
Qr	Query the volatile (RAM) memory storage. These are the values currently output by the 1940A and will only equal the values from "Qe" if no changes have been made in the settings. See manual for details of returned information.
C	Same as "Reset All" command. Restores factory defaults and clears EEPROM valid flag.
Ax N	Set Attenuation. x=a or b, depending upon which attenuation is set. N=0, 1, 2, 3, 4, 5, 6 for 0dB to 60dB attenuation.
S	Saves current state into EEPROM and sets valid flag. State used as default upon next power up or reset. Use the "Reset All" or "C" command to return to factory default values. Automatically sets EEPROM valid flag and overrides the legacy "P" command.

Model 1940A Rear Panel



POWER IN

FUSE

0-60dB

4dBm

GROUP 0
A = Frequency A
B = Frequency B

0-60dB

4dBm

GROUP 1
A = Frequency A
B = Frequency B

Coaxial

Frequency Mixer WIDE BAND

ZX05-73L+

Level 4 (LO Power +4 dBm) 2400 to 7000 MHz

CASE STYLE: FL905

Connectors	Model	Price	Qty.
SMA	ZX05-73L-S+	$48.95	(1-24)

+ RoHS compliant in accordance with EU Directive (2002/95/EC)

The +Suffix has been added in order to identify RoHS Compliance. See our web site for RoHS Compliance methodologies and qualifications.

Maximum Ratings

Operating Temperature	-40°C to 85°C
Storage Temperature	-55°C to 100°C
RF Power	50mW

Coaxial Connections

LO	2
RF	3
IF	1

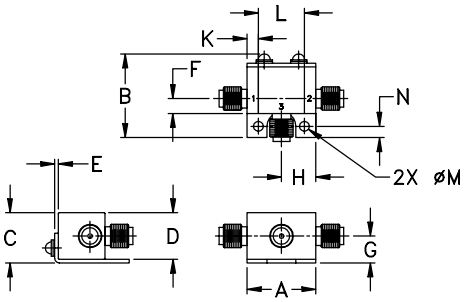
Features

- wide bandwidth, 2400 to 7000 MHz
- low conversion loss, 6.2 dB typ.
- high L-R isolation, 30 dB typ.
- excellent IF BW, DC to 3000 MHz
- rugged construction
- small size
- useable as up and down converter
- protected by US patents, 6,790,049 and 7,027,795

Applications

- satellite up and down converters
- defense radar and communications
- line of sight links
- WIFI
- blue tooth
- VSAT
- ISM

Outline Drawing



Outline Dimensions (inch / mm)

A	B	C	D	E	F	G
.74	.90	.54	.50	.04	.16	.29
18.80	22.86	13.72	12.70	1.02	4.06	7.37

H	J	K	L	M	N	wt
.37	--	.122	.496	.106	.122	grams
9.40	--	3.10	12.60	2.69	3.10	20.0

Electrical Specifications

FREQUENCY (MHz)		CONVERSION LOSS* (dB)			LO-RF ISOLATION (dB)		LO-IF ISOLATION (dB)		IP3 at center band (dBm)
LO/RF f_L-f_U	IF	Typ.	σ	Max.	Typ.	Min.	Typ.	Min.	Typ.
2400-7000	**DC-3000**								
2400-3200		6.6	0.1	8.3	33	27	20	16	10
3200-4200		6.1	0.1	8.2	30	26	26	21	12
4200-7000		6.0	0.2	8.3	23	16	18	12	9

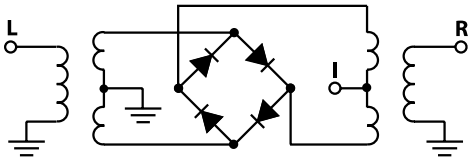
1 dB COMPR.: +1 dBm typ.

* Conversion loss at 30 MHz IF. σ is a measure of repeatability from unit to unit.

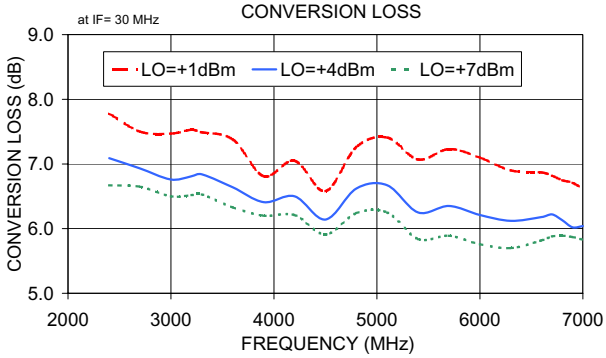
Typical Performance Data

Frequency (MHz)		Conversion Loss (dB)	Isolation L-R (dB)	Isolation L-I (dB)	VSWR RF Port (:1)	VSWR LO Port (:1)
RF	LO	LO +4dBm	LO +4dBm	LO +4dBm	LO +4dBm	LO +4dBm
2400.10	2430.10	7.09	36.72	18.75	2.91	2.80
2700.10	2730.10	6.93	33.49	21.40	3.11	1.79
3000.10	3030.10	6.76	30.70	23.16	3.15	1.87
3200.10	3230.10	6.81	30.48	25.44	3.26	1.91
3300.10	3330.10	6.84	30.61	26.57	3.35	2.00
3600.10	3630.10	6.64	30.53	28.14	2.76	2.24
3900.10	3930.10	6.41	31.12	31.02	2.57	1.94
4200.10	4230.10	6.50	28.90	28.74	3.00	1.84
4500.10	4530.10	6.14	26.88	19.45	2.62	1.93
4800.10	4830.10	6.62	26.76	14.66	2.81	2.09
5100.10	5130.10	6.67	25.23	14.59	3.00	2.38
5400.10	5430.10	6.25	23.60	15.75	2.60	2.75
5700.10	5730.10	6.35	22.83	17.68	2.39	2.95
6000.10	6030.10	6.21	21.59	20.51	2.28	2.76
6300.10	6330.10	6.12	20.54	24.64	2.21	2.18
6600.10	6630.10	6.18	19.39	26.49	2.25	1.54
6700.10	6730.10	6.22	19.20	26.64	2.17	1.37
6800.10	6830.10	6.13	19.15	26.57	2.01	1.25
6900.10	6930.10	6.02	18.83	27.11	1.84	1.13
7000.10	7030.10	6.04	18.34	26.85	1.86	1.05

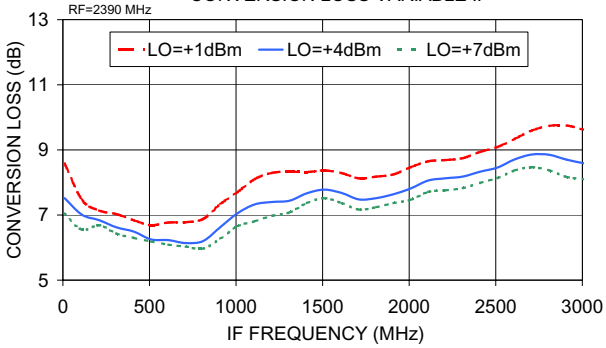
Electrical Schematic



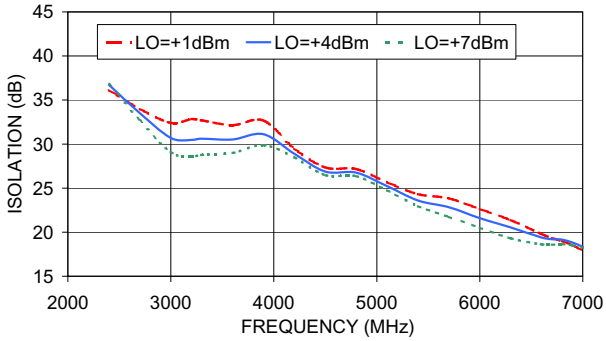
ZX05-73L+
CONVERSION LOSS



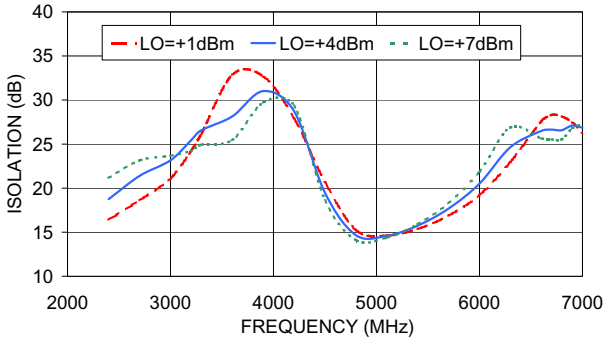
ZX05-73L+
CONVERSION LOSS VARIABLE IF



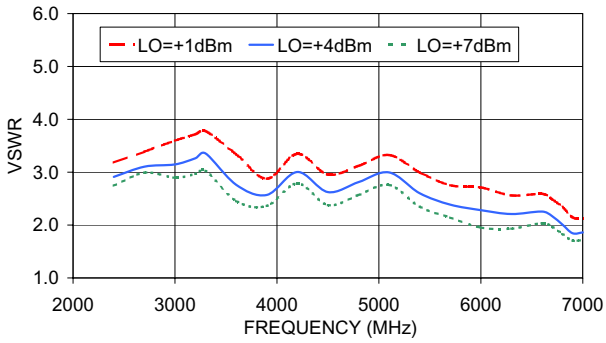
ZX05-73L+
L-R ISOLATION



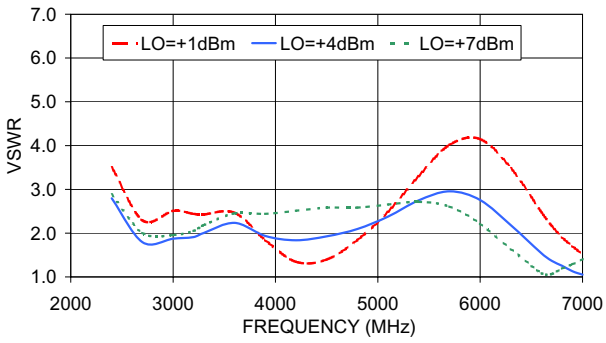
ZX05-73L+
L-I ISOLATION



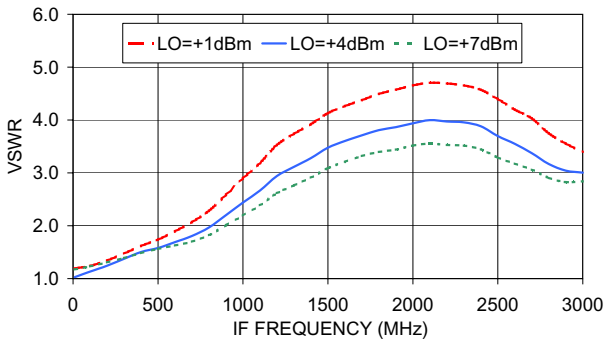
ZX05-73L+
RF VSWR



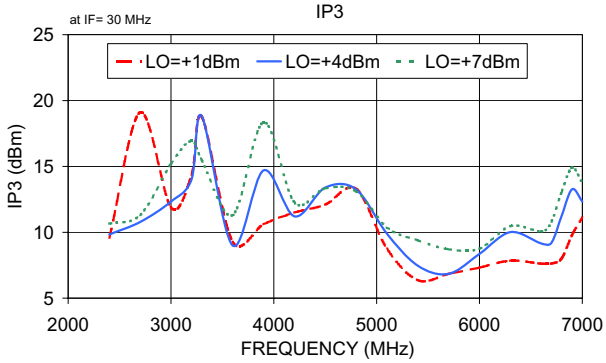
ZX05-73L+
LO VSWR



ZX05-73L+
IF VSWR



ZX05-73L+
IP3



Technical Sales
Italy
02 41309.1 (Milano), 06 520871 (Roma)
ni.italy@ni.com

NI PCI-6284

18-Bit, 500 kS/s (Multichannel), 625 kS/s (1-Channel), 32 Analog Inputs

- 48 digital I/O; two 32-bit, 80 MHz counters; analog and digital triggering
- Correlated DIO (32 clocked lines, 10 MHz)
- Programmable 40 kHz lowpass filters
- NI-MCal calibration technology for increased measurement accuracy
- NIST-traceable calibration certificate and more than 70 signal conditioning options
- NI-DAQmx driver software and NI LabVIEW SignalExpress interactive data-logging software

Overview

The National Instruments PCI-6284 is a high-accuracy multifunction M Series data acquisition (DAQ) board optimized for 18-bit analog input accuracy. This resolution is equivalent to 5½ digits for DC measurements. To ensure accuracy, the NI-PGIA 2 amplifier technology is optimized for high linearity and fast settling to 18 bits, and programmable lowpass filters reject high-frequency noise and prevent aliasing.

High-accuracy M Series devices feature programmable offsets and references on the analog output channels to obtain maximum 16-bit resolution on any custom signal. High-accuracy M Series multifunction DAQ devices are ideal for applications including device test and characterization, and for sensor and signal measurements requiring instrument-class accuracy. To learn more about M Series technologies, device specifications, and information on recommended cables and accessories, please refer to the data sheet and specifications.

Driver Software

M Series devices work with multiple operating systems using three driver software options including NI-DAQmx, NI-DAQmx Base, and the Measurement Hardware DDK. Browse the information in the Resources tab to learn more about driver software or download a driver. M Series devices are not compatible with the Traditional NI-DAQ (Legacy) driver.

Application Development Environments

With NI LabVIEW, you can create custom data acquisition applications with the ease of graphical programming and power of more than 500 analysis functions and advanced programming tools. LabVIEW Full and Professional Development Systems include LabVIEW SignalExpress for interactive data logging. M Series data acquisition devices are compatible with the following versions (or later) of NI application software – LabVIEW 7.x, LabWindows™/CVI 7.x, or Measurement Studio 7.x; LabVIEW SignalExpress 1.x; or LabVIEW with the LabVIEW Real-Time Module 7.1. M Series data acquisition devices are also compatible with Visual Studio .NET, C/C++, and Visual Basic 6.

Specifications

Specifications Documents

- Detailed Specifications

- Data Sheet

Specifications Summary

General	
Form Factor	PCI
OS Support	Windows, Real-Time, Linux, Mac OS
Measurement Type	Digital, Frequency, Quadrature encoder, Voltage
DAQ Product Family	M Series
LabVIEW RT Support	Yes
Analog Input	
Number of Channels	32 SE/16 DI
Sample Rate	625 kS/s
Resolution	18 bits
Simultaneous Sampling	No
Maximum Voltage Range	-10..10 V
Range Accuracy	980 µV
Range Sensitivity	24 µV
Minimum Voltage Range	-100..100 mV
Range Accuracy	28 µV
Range Sensitivity	0.8 µV
Number of Ranges	7
On-Board Memory	4095 samples
Signal Conditioning	Low-pass filtering
Analog Output	
Number of Channels	0
Digital I/O	
Number of Channels	48 DIO
Timing	Hardware, Software
Maximum Clock Rate	10 MHz
Logic Levels	TTL
Maximum Input Range	0..5 V
Maximum Output Range	0..5 V
Input Current Flow	Sinking, Sourcing

Programmable Input Filters	Yes
Output Current Flow	Sinking, Sourcing
Current Drive (Channel/Total)	24 mA/1 A
Watchdog Timer	No
Supports Programmable Power-Up States?	Yes
Supports Handshaking I/O?	No
Supports Pattern I/O?	Yes
Counter/Timers	
Number of Counter/Timers	2
Resolution	32 bits
Maximum Source Frequency	80 MHz
Minimum Input Pulse Width	12.5 ns
Logic Levels	TTL
Maximum Range	0..5 V
Timebase Stability	50 ppm
GPS Synchronization	No
Pulse Generation	Yes
Buffered Operations	Yes
Debouncing/Glitch Removal	Yes
Number of DMA Channels	2
Timing/Triggering/Synchronization	
Synchronization Bus (RTSI)	Yes
Triggering	Analog, Digital
Physical Specifications	
Length	15.5 cm
Width	9.7 cm
I/O Connector	68-pin VHDCI female

Pricing

Step 1: Verify Device and Quantity Selection

Part	Description	Est Ship Days	US Dollars*	Qty

Number			
779110-01	NI PCI-6284	--	For price, select country

Each NI PCI-6284 requires: 2 Cables, 2 Connector Blocks

NI PCI-6284 Cable Connector Block

Step 2: Select Cable

Part Number	Description	Est Ship Days	US Dollars*	Qty
Connector 0				
Shielded				
192061-02	SHC68-68-EPM Cable (2m) NI Recommended	--	For price, select country	
192061-01	SHC68-68-EPM Cable (1m)	--	For price, select country	
192061-0R5	SHC68-68-EPM Cable (0.5m)	--	For price, select country	
192061-10	SHC68-68-EPM Cable (10m)	--	For price, select country	
Unshielded				
187252-01	RC68-68 Cable (1m)	--	For price, select country	
187252-0R5	RC68-68 Cable (0.5m)	--	For price, select country	
187252-0R25	RC68-68 Cable (0.25m)	--	For price, select country	
Connector 1				
Shielded				
192061-02	SHC68-68-EPM Cable (2m) NI Recommended	--	For price, select country	
192061-01	SHC68-68-EPM Cable (1m)	--	For price, select country	
192061-0R5	SHC68-68-EPM Cable (0.5m)	--	For price, select country	
192061-10	SHC68-68-EPM Cable (10m)	--	For price,	

			select country
Unshielded			
187252-01	RC68-68 Cable (1m)	--	For price, select country
187252-0R5	RC68-68 Cable (0.5m)	--	For price, select country
187252-0R25	RC68-68 Cable (0.25m)	--	For price, select country

Step 3: Select Connector Block

Part Number	Description	Est Ship Days	US Dollars*	Qty
Connector 0				
Screw Terminals				
776844-01	SCB-68 - Shielded NI Recommended	--	For price, select country	
BNC Termination				
777643-01	BNC-2110 - Shielded	--	For price, select country	
777960-01	BNC-2120 - Shielded	--	For price, select country	
779556-01	BNC-2090A - Shielded, Rack Mountable	--	For price, select country	
Screw Terminals				
779475-01	SCC-68 - Unshielded	--	For price, select country	
777141-01	TBX-68 Unshielded, I/O Connector Block with DIN-Rail Mounting - Unshielded	--	For price, select country	
777145-01	CB-68LP - Unshielded	--	For price, select country	
777145-02	CB-68LPR - Unshielded	--	For price, select country	
Connector 1				
Screw Terminals				
776844-01	SCB-68 - Shielded NI Recommended	--	For price, select country	
BNC Termination				
777643-01	BNC-2110 - Shielded	--	For price, select country	

777960-01	BNC-2120 - Shielded	--	For price, select country
779556-01	BNC-2090A - Shielded, Rack Mountable	--	For price, select country
Screw Terminals			
779475-01	SCC-68 - Unshielded	--	For price, select country
777141-01	TBX-68 Unshielded, I/O Connector Block with DIN-Rail Mounting - Unshielded	--	For price, select country
777145-01	CB-68LP - Unshielded	--	For price, select country
777145-02	CB-68LPR - Unshielded	--	For price, select country

* You have selected Italy as the country where you will use the product(s). Pricing may have changed since you printed this document on 02/02/2009. Please visit *ni.com* to see current pricing.

Step 4: Place Order or Obtain Quote

Order Online or by Fax

1 . Navigate to *ni.com/products* and select "Order by Part Number" found under the "Business Center" section.
2 . Once you have added your items to your cart, see the "Your Cart Options" section to place your order, obtain a quote, or print a fax form.

Order by Phone

Call 02 41309.1 (Milano), 06 520871 (Roma) to place your order or obtain a quote.

Software

Application Need

Data acquisition, analysis, and user interface customization	Data logging
Automated test and test sequencing	Simulation and control design
Industrial monitoring and control	

Graphical Programming

Select any of the following software products

Part Number	Description	Est Ship Days	US Dollars*	Qty
LabVIEW Software				
776670-09	NI LabVIEW Full Development System for Windows (English) NI Recommended	--	For price, select country	
777756-09	NI LabVIEW Full Development System for	--	For price, select country	

	Linux			
776675-01	LabVIEW Application Builder for Windows (English) NI Recommended	--	For price, select country	
777755-03	NI LabVIEW Application Builder for Linux	--	For price, select country	
778406-03	NI LabVIEW Report Generation Toolkit for Microsoft Office	--	For price, select country	
Specialty Software				
778807-09	DIAdem Advanced Edition (English)	--	For price, select country	

Text-Based Programming

Select any of the following software products

Part Number	Description	Est Ship Days	US Dollars*	Qty
Application Software				
776800-09	LabWindows/CVI Full Development System for Windows	--	For price, select country	
778801-09	NI Measurement Studio Professional Edition for Microsoft Visual Studio	--	For price, select country	
779384-03	NI LabWindows/CVI Run-Time Module for Linux	--	For price, select country	
Specialty Software				
778807-09	DIAdem Advanced Edition (English)	--	For price, select country	

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Features

- **Supply Voltage 5V**
- **Very Low Power Consumption 125 mW**
- **Very Good Image Rejection By Means of Phase Control Loop for Precise 90° Phase Shifting**
- **Duty-cycle Regeneration for Single-ended LO Input Signal**
- **Low LO Input Level –10 dBm**
- **LO Frequency from 70 MHz to 1 GHz**
- **Power-down Mode**
- **25 dB Gain Control**
- **Very Low I/Q Output DC Offset Voltage Typically < 5 mV**

Benefits

- **Low Current Consumption**
- **Easy to Implement**
- **Perfect Performance for Large Variety of Wireless Applications**

Electrostatic sensitive device.
Observe precautions for handling.

1000-MHz Quadrature Demodulator

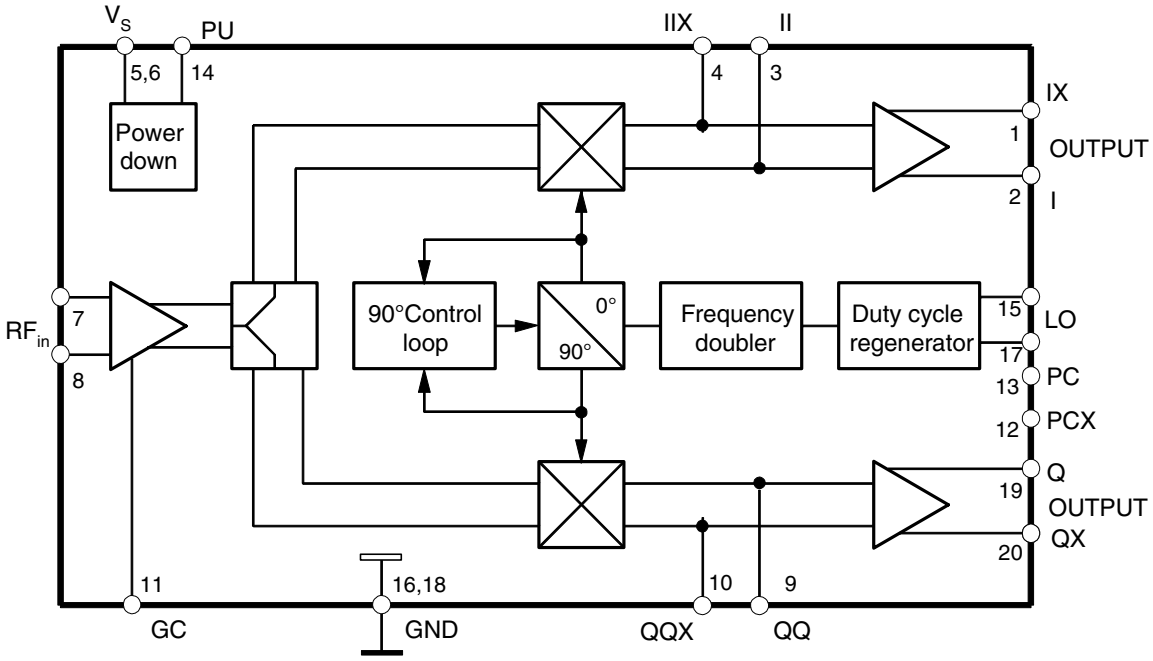
U2794B

1. Description

The silicon monolithic integrated circuit U2794B is a quadrature demodulator manufactured using Atmel®'s advanced UHF technology. This demodulator features a frequency range from 70 MHz to 1000 MHz, low current consumption, selectable gain, power-down mode and adjustment-free handling. The IC is suitable for direct conversion and image rejection applications in digital radio systems up to 1 GHz such as cellular radios, cordless telephones, cable TV and satellite TV systems.

4653E–CELL–07/06

Figure 1-1. Block Diagram



2. Pin Configuration

Figure 2-1. Pinning SSO20

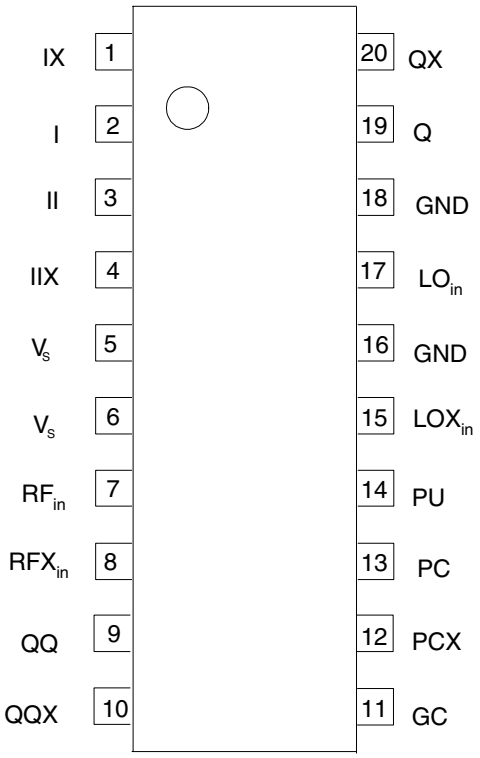


Table 2-1. Pin Description

Pin	Symbol	Function
1	IX	IX output
2	I	I output
3	II	II lowpass filter I
4	IIX	IIX lowpass filter I
5	V_S	Supply voltage
6	V_S	Supply voltage
7	RF_{in}	RF input
8	RFX_{in}	RFX input
9	QQ	QQ lowpass filter Q
10	QQX	QQX lowpass filter Q
11	GC	GC gain control
12	PCX	PCX phase control
13	PC	PC phase control
14	PU	PU power up
15	LOX_{in}	LOX input
16	GND	Ground
17	LO_{in}	LO input
18	GND	Ground
19	Q	Q output
20	QX	QX output

3. Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameters	Symbol	Value	Unit
Supply voltage	V_S	6	V
Input voltage	V_i	0 to V_S	V
Junction temperature	T_j	+125	°C
Storage-temperature range	T_{stg}	–55 to +125	°C

4. Thermal Resistance

Parameters	Symbol	Value	Unit
Junction ambient SSO20	R_{thJA}	140	K/W

5. Operating Range

Parameters	Symbol	Value	Unit
Supply-voltage range	V_S	4.75 to 5.25	V
Ambient-temperature range	T_{amb}	–40 to +85	°C

6. Electrical Characteristics

Test conditions (unless otherwise specified); V_S = 5V, T_{amb} = 25°C, referred to test circuit
System impedance Z_O = 50Ω, f_{iLO} = 950 MHz, P_{iLO} = –10 dBm

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
1.1	Supply-voltage range		5, 6	V_S	4.75		5.25	V	A
1.2	Supply current		5, 6	I_S	22	30	35	mA	A
2	**Power-down Mode**								
2.1	"OFF" mode supply current	$V_{PU} \leq$ 0.5V V_{PU} = 1.0 V(1)	14, 5 6	I_{SPU}		≤ 1 20		µA µA	B D
3	**Switch Voltage**								
3.1	"Power ON"		14	V_{PON}	4			V	D
3.2	"Power DOWN"		14	V_{POFF}			1	V	D
4	**LO Input, LO_{in}**								
4.1	Frequency range		17	f_{iLO}	70		1000	MHz	D
4.2	Input level	(2)	17	P_{iLO}	–12	–10	–5	dBm	D
4.3	Input impedance	See Figure 6-10	17	Z_{iLO}		50		Ω	D
4.4	Voltage standing wave ratio	See Figure 6-3	17	$VSWR_{LO}$		1.2	2		D
4.5	Duty-cycle range		17	DCR_{LO}	0.4		0.6		D
5	**RF Input, RF_{in}**								
5.1	Noise figure (DSB) symmetrical output	at 950 MHz(3) at 100 MHz	7, 8	NF		12 10		dB	D
5.2	Frequency range	$f_{iRF} = f_{iLO} \pm BW_{YQ}$	7, 8	f_{iRF}	40		1030	MHz	D
5.3	–1 dB input compression point	High gain Low gain	7, 8	P_{1dBHG} P_{1dBLG}		–8 +3.5		dBm	D
5.4	Second order IIP	(4)	7, 8	IIP_{2HG}		35		dBm	D
5.5	Third order IIP	High gain Low gain	7, 8	IIP_{3HG} IIP_{3LG}		+3 +13		dBm	D
5.6	LO leakage	Symmetric input Asymmetric input	7, 8	L_{OL}		≤ –60 ≤ –55		dBm	D
5.7	Input impedance	see Figure 6-10	7, 8	Z_{iRF}		500II0.8		ΩIIpF	D

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Notes:
1. During power-down status a load circuitry with DC-isolation to GND is assumed, otherwise a current of I ≈ (VS –0.8V)/RI has to be added to the above power-down current for each output I, IX, Q, QX.
2. The required LO-Level is a function of the LO frequency (see Figure 6-6).
3. Measured with input matching. For 950 MHz, the optional transmission line T3 at the RF input may be used for this purpose. Noise figure measurements without using the differential output signal result in a worse noise figure.
4. Using pins 7 and 8 as a symmetric RF input, the second-order IIP can be improved.
5. Due to test board parasitics, this bandwidth may be reduced and not be equal for I, IX, Q, QX. If symmetry and full bandwidth is required, the lowpass pins 3, 4 and 9, 10 should be isolated from the board. the bandwidth of the I/Q outputs can be increased further by using a resistor between pins 3, 4, 9 and 10. These resistors shunt the internal loads of RI ~ 5.4 kΩ. The decrease in gain here has to be considered.
6. The internal current of the output emitter followers is 0.6 mA. This reduces the undistorted output voltage swing at a 50Ω load to approximately 30 mV. For low signal distortion the load impedance should be RI ≥ 5 kΩ
7. Referred to the level of the output vector $\sqrt{I^2 + Q^2}$
8. The low-gain status is achieved with an open or high-ohmic pin 11. A recommended application circuit for switching between high and low gain status is shown in Figure 6-1.

6. Electrical Characteristics (Continued)

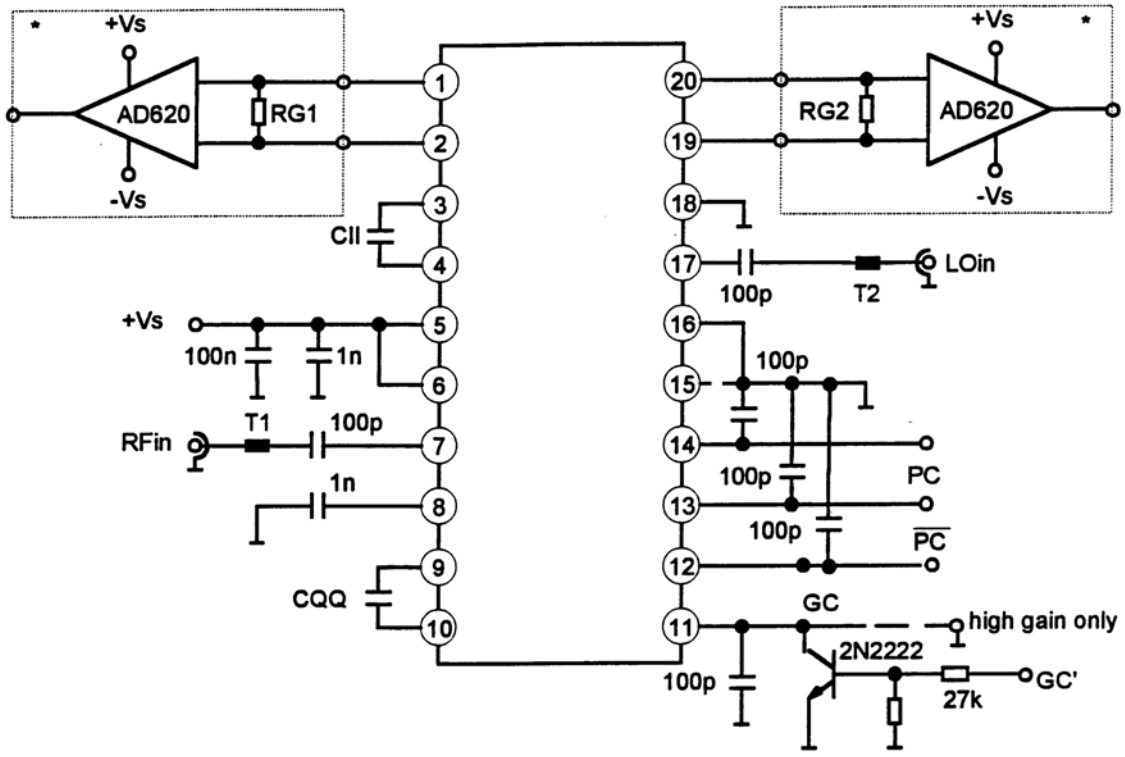
Test conditions (unless otherwise specified); V_S = 5V, T_{amb} = 25°C, referred to test circuit
System impedance Z_O = 50Ω, f_{iLO} = 950 MHz, P_{iLO} = –10 dBm

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
6	**I/Q Outputs (I, IX, Q, QX) Emitter Follower I = 0.6 mA**								
6.1	3-dB bandwidth w/o external C		1, 2, 19, 20	BWI/Q	≥ 30			MHz	D
6.2	I/Q amplitude error		1, 2, 19, 20	Ae	–0.5	≤ ±0.2	+0.5	dB	B
6.3	I/Q phase error		1, 2, 19, 20	Pe	–3	≤ ±1.5	+3	Deg	B
6.4	I/Q maximum output swing	Symm. output R_L > 5 kΩ	1, 2, 19, 20	V_{PP}			2		D
6.5	DC output voltage		1, 2, 19, 20	V_{OUT}	2.5	2.8	3.1	V	A
6.6	DC output offset voltage	(6)	1, 2, 19, 20	V_{offset}		< 5		mV	Test spec.
6.7	Output impedance	see Figure 6-10	1, 2, 19, 20	Z_{out}		50		Ω	D
7	**Gain Control, GC**								
7.1	Control range power Gain high Gain low	(7)	11	GCR G_H G_L		25 23 –2		dB dBm dBm	D B D
7.2	**Switch Voltage**								
7.3	“Gain high”		11				1	V	
7.4	“Gain low”	(8)	11 < open						
7.5	**Settling Time, ST**								
7.6	Power “OFF” - “ON”			T_{SON}		< 4		µs	D
7.7	Power “ON” - “OFF”			T_{SOFF}		< 4		µs	D

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Notes:
1. During power-down status a load circuitry with DC-isolation to GND is assumed, otherwise a current of I ≈ (VS –0.8V)/RI has to be added to the above power-down current for each output I, IX, Q, QX.
2. The required LO-Level is a function of the LO frequency (see Figure 6-6).
3. Measured with input matching. For 950 MHz, the optional transmission line T3 at the RF input may be used for this purpose. Noise figure measurements without using the differential output signal result in a worse noise figure.
4. Using pins 7 and 8 as a symmetric RF input, the second-order IIP can be improved.
5. Due to test board parasitics, this bandwidth may be reduced and not be equal for I, IX, Q, QX. If symmetry and full bandwidth is required, the lowpass pins 3, 4 and 9, 10 should be isolated from the board. the bandwidth of the I/Q outputs can be increased further by using a resistor between pins 3, 4, 9 and 10. These resistors shunt the internal loads of RI ~ 5.4 kΩ The decrease in gain here has to be considered.
6. The internal current of the output emitter followers is 0.6 mA. This reduces the undistorted output voltage swing at a 50Ω load to approximately 30 mV. For low signal distortion the load impedance should be RI ≥ 5 kΩ
7. Referred to the level of the output vector $\sqrt{I^2 + Q^2}$
8. The low-gain status is achieved with an open or high-ohmic pin 11. A recommended application circuit for switching between high and low gain status is shown in Figure 6-1.

Figure 6-1. Test Circuit



* optional for single-ended tests (notice 3 dB bandwidth of AD620)
T1, T2 = transmission line $Z_O = 50\Omega$
If no GC function is required, connect Pin 11 to GND.
For high and low gain status GC´ is to be switched to GND respectively to V_S.

Figure 6-2. I and Q phase for $f_{RF} > f_{LO}$. For $f_{RF} < f_{LO}$ the phase is inverted.

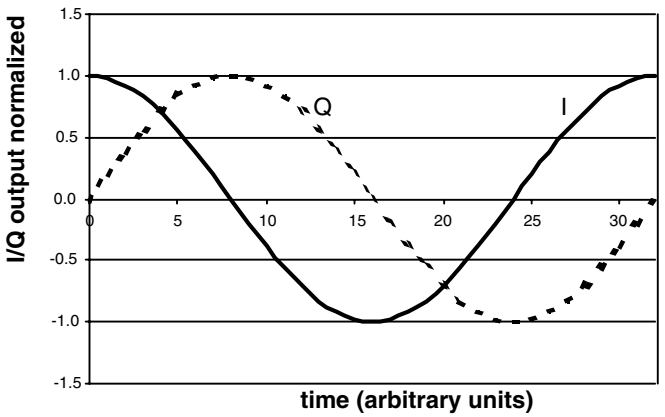


Figure 6-3. Typical VSWR Frequency Response of the LO Input

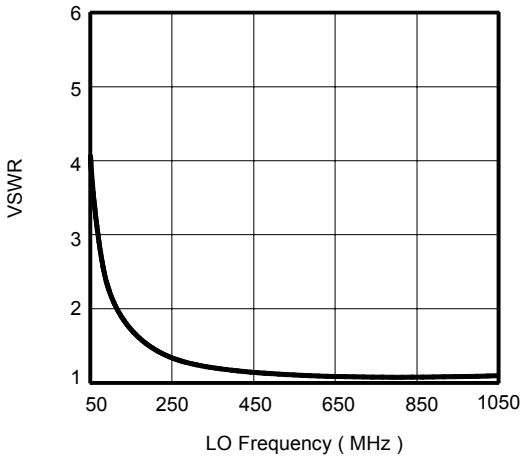


Figure 6-4. Noise Figure versus LO Frequency; o: Value at 950 MHz with RF Input Matching with T3

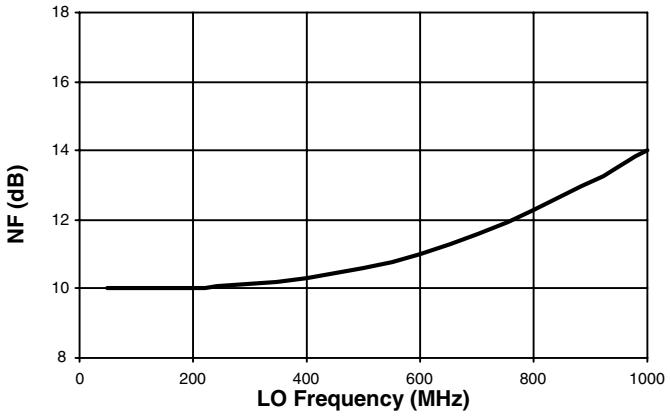


Figure 6-5. Typical Suitable LO Power Range versus Frequency

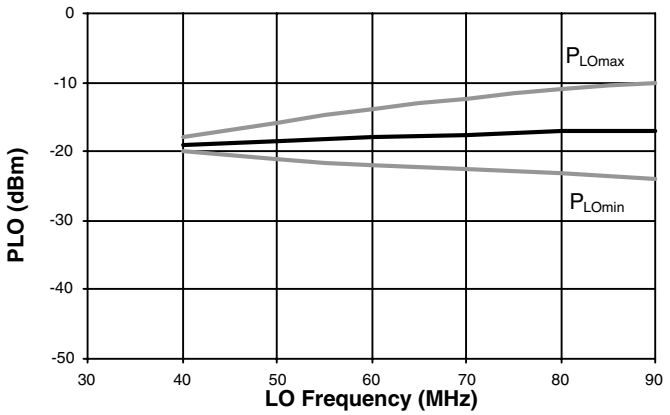


Figure 6-6. Gain versus LO Frequency; x: Value at 950 MHz with RF Input Matching with T3

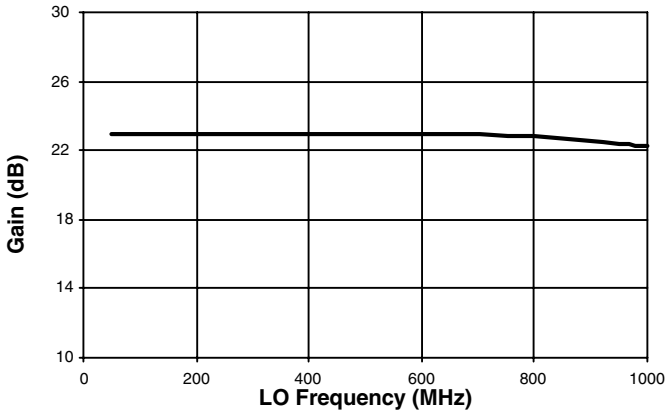


Figure 6-7. Typical Output Signal versus LO Frequency for P_{RF} = –15 dBm and PLO = –15 dBm

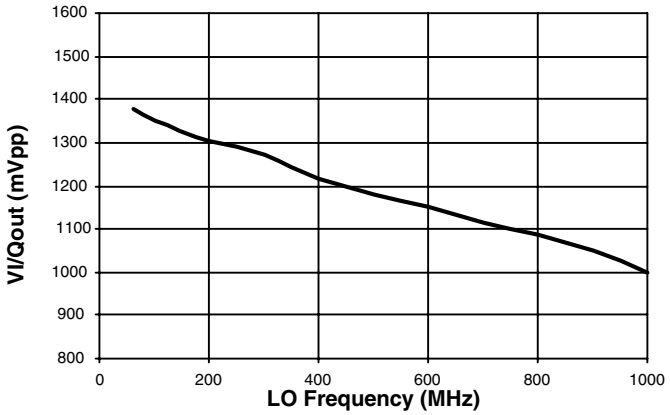


Figure 6-8. Typical Suitable LO Power Range versus Frequency

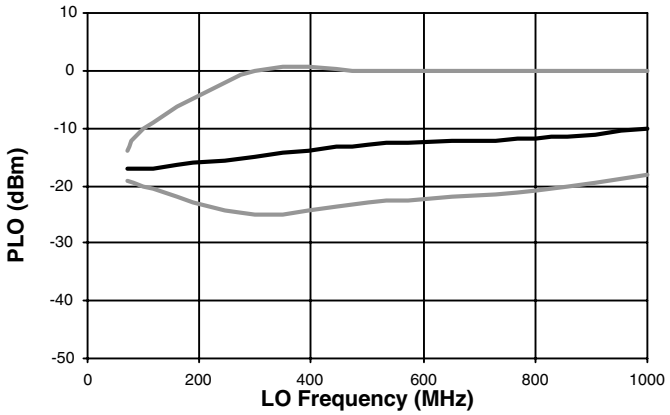


Figure 6-9. Typical Output Voltage (single ended) versus P_{RF} at T_{amb} = 25°C and PLO = –15 dBm

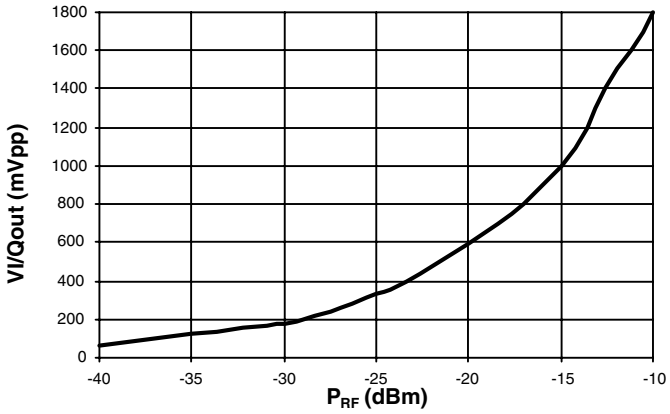
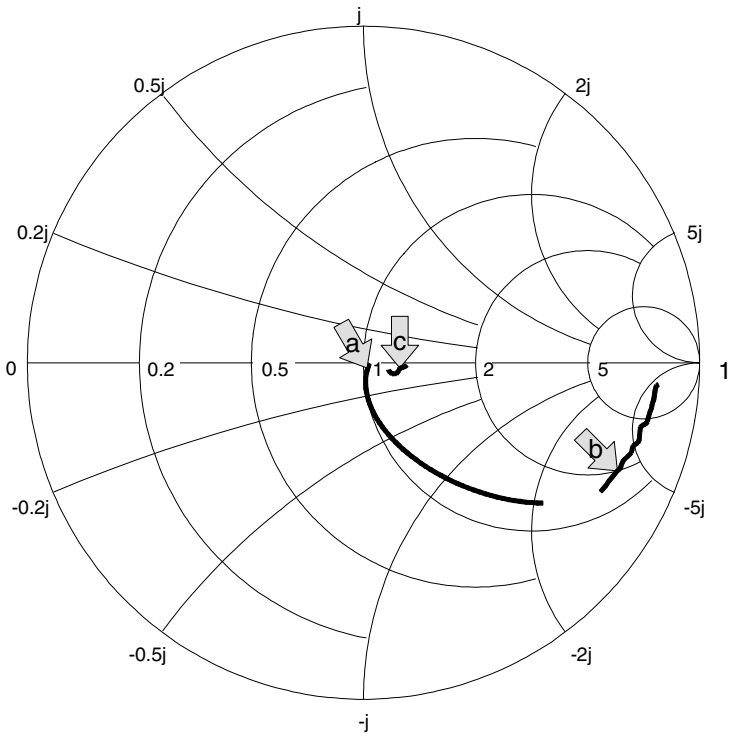


Figure 6-10. Typical S11 Frequency Response



a: LO input, LO frequency from 100 MHz to 1100 MHz, marker: 950 MHz
b: RF input, RF frequency from 100 MHz to 1100 MHz, marker: 950 MHz
c: I/Q Outputs, Baseband Frequency from 5 MHz to 55 MHz, marker: 25 MHz

Figure 6-11. Evaluation Board Layout

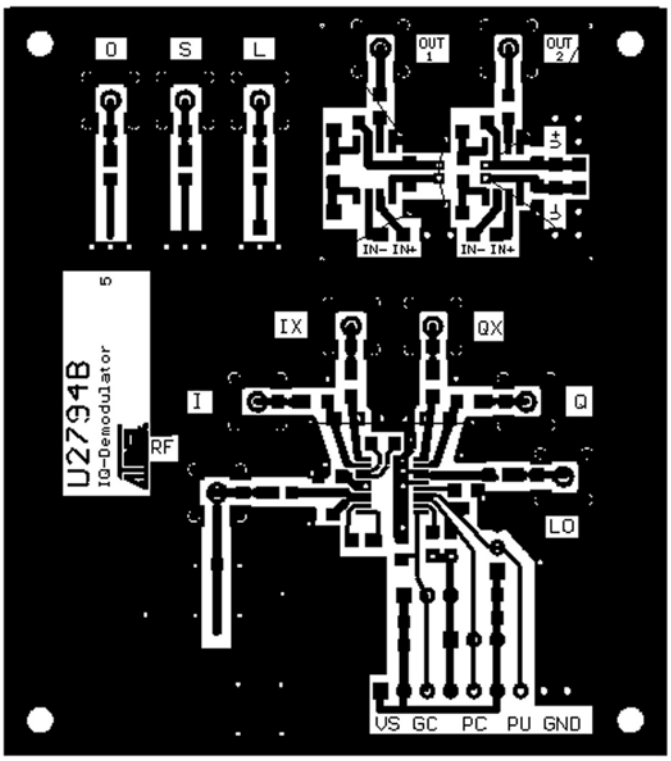
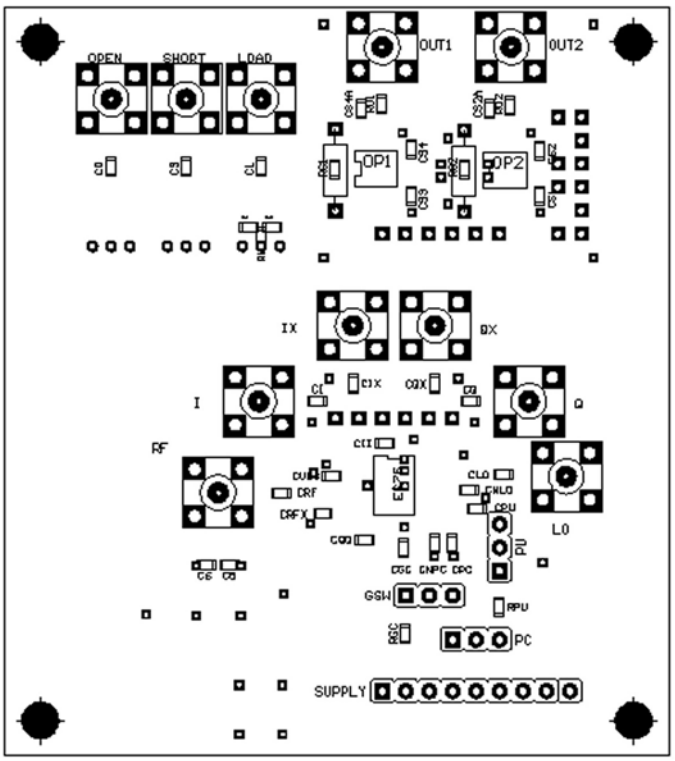


Figure 6-12. Evaluation Board



6.1 External Components

CUCC	100 nF	
CRFX	1 nF	
CLO	100 pF	
CNLO	1 nF	
CRF	100 pF	
CII, CQQ		optional external lowpass filters
T3		transmission line for RF-input matching, to connect optionally
CI, CIX		optional for AC-coupling at
CQ, CQX		baseband outputs
CPDN	100 pF	not connected
CGC	100 pF	
CPC	100 pF	not connected
CNPC	100 pF	not connected
GSW		gain switch

6.2 Calibration Part

CO, CS, CL	100 pF
RL	50Ω

6.3 Conversion to Single Ended Output

(see datasheet of AD620)

OP1, OP2		AD620
RG1, RG2		prog. gain, see datasheet, for 5.6 kΩ a gain of 1 at 50Ω is achieved together with RD1 and RD2.
RD1, RD2	450Ω	
CS1, CS2	100 nF	
CS3, CS4	100 nF	

7. Description of the Evaluation Board

Board material: epoxy; $\varepsilon r = 4.8$, thickness = 0.5 mm, transmission lines: $Z_O = 50\Omega$

The board offers the following functions:

- Test circuit for the U2794B:
  - The supply voltage and the control inputs GC, PC and PU are connected via a plug strip. The control input voltages can be generated via external potentiometers; then the inputs should be AC-grounded (time requirements in burst mode for power up have to be considered).
  - The outputs I, IX, Q, QX are DC coupled via an plug strip or can be AC-connected via SMB plugs for high frequency tests e.g. noise figure or s-parameter measurement. The Pins II, IIX, QQ, QQX allow user-definable filtering with 2 external capacitors CII, CQQ.
  - The offsets of both channels can be adjusted with two potentiometers or resistors.
  - The LO- and the RF-inputs are AC-coupled and connected via SMB plugs. If transmission line T3 is connected to the RF-input and AC-grounded at the other end, gain and noise performance can be improved (input matching to 50Ω).
  - The complementary RF-input is AC-coupled to GND (CRFX = 1 nF), the same appears to the complementary LO input (CNLO = 1 nF).
- A calibration part which allows to calibrate an s-parameter analyzer directly to the in- and output- signal ports of the U2794B.
- For single-ended measurements at the demodulator outputs, two OPs (e.g., AD620 or other) can be configured with programmable gain; together with an output-divider network RD = 450Ω to RL = 50Ω, direct measurements with 50Ω load impedances are possible at frequencies t < 100 kHz.

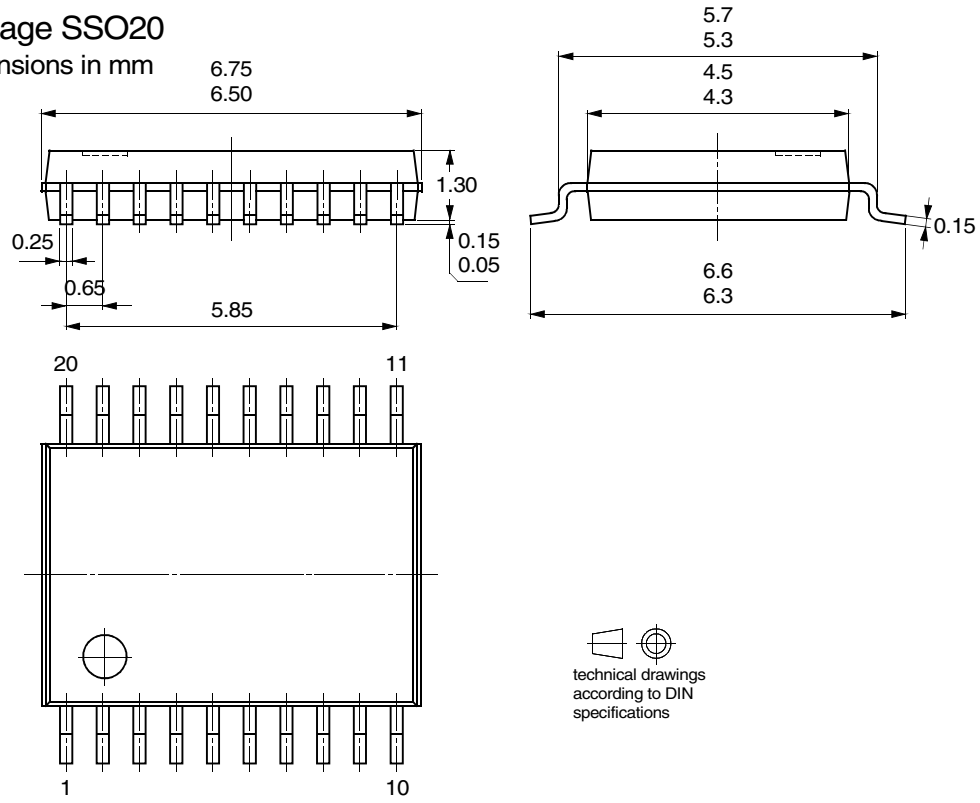
8. Ordering Information

Extended Type Number	Package	Remarks
U2794B-NFSH	SSO20	Tube, MOQ 830 pcs, Pb-free
U2794B-NFSG3H	SSO20	Taped and reeled, MOQ 4000 pcs, Pb-free

9. Package Information

Package SSO20

Dimensions in mm



10. Revision History

Please note that the following page numbers referred to in this section refer to the specific revision mentioned, not to this document.

Revision No.	History
4653E-CELL-07/06	• Page 4, Abs. Max. Ratings table: Storage temperature values changed • Put datasheet in a new template

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50 MHz to 1000 MHz Quadrature Demodulator

AD8348

FEATURES

Integrated I/Q demodulator with IF VGA amplifier
Operating IF frequency 50 MHz to 1000 MHz
(3 dB IF BW of 500 MHz driven from R_S = 200 Ω)
Demodulation bandwidth 75 MHz
Linear-in-decibel AGC range 44 dB
Third-order intercept
IIP3 +28 dBm @ minimum gain (F_{IF} = 380 MHz)
IIP3 −8 dBm @ maximum gain (F_{IF} = 380 MHz)
Quadrature demodulation accuracy
Phase accuracy 0.5°
Amplitude balance 0.25 dB
Noise figure 11 dB @ maximum gain (F_{IF} = 380 MHz)
LO input −10 dBm
Single supply 2.7 V to 5.5 V
Power-down mode
Compact, 28-lead TSSOP package

APPLICATIONS

QAM/QPSK demodulator
W-CDMA/CDMA/GSM/NADC
Wireless local loop
LMDS

FUNCTIONAL BLOCK DIAGRAM

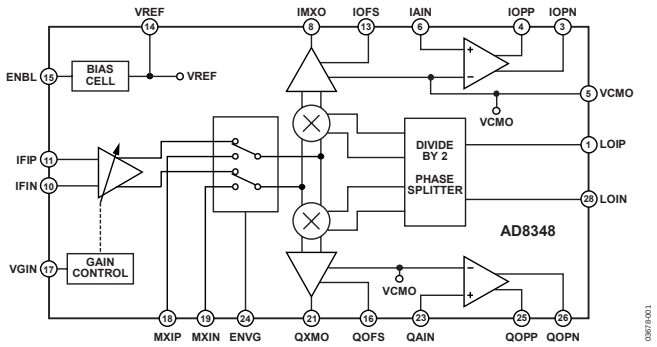

Figure 1.

GENERAL DESCRIPTION

The AD8348 is a broadband quadrature demodulator with an integrated intermediate frequency (IF), variable gain amplifier (VGA), and integrated baseband amplifiers. It is suitable for use in communications receivers, performing quadrature demodulation from IF directly to baseband frequencies. The baseband amplifiers are designed to interface directly with dual-channel ADCs, such as the AD9201, AD9283, and AD9218, for digitizing and post-processing.

The IF input signal is fed into two Gilbert cell mixers through an X-AMP® VGA. The IF VGA provides 44 dB of gain control. A precision gain control circuit sets a linear-in-decibel gain characteristic for the VGA and provides temperature compensation. The LO quadrature phase splitter employs a divide-by-2 frequency divider to achieve high quadrature accuracy and amplitude balance over the entire operating frequency range.

Optionally, the IF VGA can be disabled and bypassed. In this mode, the IF signal is applied directly to the quadrature mixer inputs via the MXIP and MXIN pins.

Separate I- and Q-channel baseband amplifiers follow the baseband outputs of the mixers. The voltage applied to the VCMO pin sets the dc common-mode voltage level at the baseband outputs. Typically, VCMO is connected to the internal VREF voltage, but it can also be connected to an external voltage. This flexibility allows the user to maximize the input dynamic range to the ADC. Connecting a bypass capacitor at each offset compensation input (IOFS and QOFS) nulls dc offsets produced in the mixer. Offset compensation can be overridden by applying an external voltage at the offset compensation inputs.

The mixers' outputs are brought off-chip for optional filtering before final amplification. Inserting a channel selection filter before each baseband amplifier increases the baseband amplifiers' signal handling range by reducing the amplitude of high level, out-of-channel interferers before the baseband signal is fed into the I/Q baseband amplifiers. The single-ended mixer output is amplified and converted to a differential signal for driving ADCs.

Rev. A

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8/03—Revision 0: Initial Version

SPECIFICATIONS

V_S = 5 V, T_A = 25°C, F_{LO} = 380 MHz, F_{IF} = 381 MHz, P_{LO} = −10 dBm, R_S (LO) = 50 Ω, R_S (IFIP and MXIP/MXIN) = 200 Ω, unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
OPERATING CONDITIONS					
LO Frequency Range	External input = 2 × LO frequency	100		2000	MHz
IF Frequency Range		50		1000	MHz
Baseband Bandwidth			75		MHz
LO Input Level	50 Ω source	−12	−10	0	dBm
V_{SUPPLY} (V_S)		2.7		5.5	V
Temperature Range		−40		+85	°C
IF FRONT END WITH VGA	IFIP to IMXO (QMXO), ENVG = 5 V, IMXO/QMXO load = 1.5 kΩ				
Input Impedance	Measured differentially across MXIP/MXIN		200||1.1		Ω||pF
Gain Control Range			44		dB
Maximum Conversion Voltage Gain	VGIN = 0.2 V (maximum voltage gain)		25.5		dB
Minimum Conversion Voltage Gain	VGIN = 1.2 V (minimum voltage gain)		−18.5		dB
3 dB Bandwidth			500		MHz
Gain Control Linearity	VGIN = 0.4 V (+21 dB) to 1.1 V (−14 dB)		±0.5		dB
IF Gain Flatness	F_{IF} = 380 MHz ± 5% (VGIN = 1.2 V)		0.1		dB p-p
	F_{IF} = 900 MHz ± 5% (VGIN = 1.2 V)		1.3		dB p-p
Input 1 dB Compression Point (P1dB)	VGIN = 0.2 V (maximum gain)		−22		dBm
	VGIN = 1.2 V (maximum gain)		+13		dBm
Second-Order Input Intercept (IIP2)	IF1 = 385 MHz, IF2 = 386 MHz				
	+3 dBm each tone from 200 Ω source, VGIN = 1.2 V (minimum gain)		65		dBm
	−42 dBm each tone from 200 Ω source, VGIN = 0.2 V (maximum gain)		18		dBm
Third-Order Input Intercept (IIP3)	IF1 = 381 MHz, IF2 = 381.02 MHz				
	Each tone 10 dB below P1dB from 200 Ω source, VGIN = 1.2 V (minimum gain)		28		dBm
	Each tone 10 dB below P1dB from 200 Ω source, VGIN = 0.2 V (maximum gain)		−8		dBm
LO Leakage	Measured at IFIP, IFIN		−80		dBm
	Measured at IMXO/QMXO (LO = 50 MHz)		−60		dBm
Demodulation Bandwidth	Small signal 3 dB bandwidth		75		MHz
Quadrature Phase Error[1]	LO = 380 MHz (LOIP/LOIN 760 MHz)	−0.7	±0.1	+0.7	Degrees
	vs. temperature		−0.0032		°/°C
	vs. baseband frequency (dc to 30 MHz)		+0.01		°/MHz
I/Q Amplitude Imbalance[1]		−0.3	±0.05	+0.3	dB
	vs. temperature		0		dB/°C
	vs. baseband frequency (dc to 30 MHz)		±0.0125		dB
Noise Figure (Double Sideband)	Maximum gain, from 200 Ω source, F_{IF} = 380 MHz		10.75		dB
Mixer Output Impedance			40		Ω
Capacitive Load	Shunt from IMXO, QMXO to VCMO	0		10	pF
Resistive Load	Shunt from IMXO, QMXO to VCMO	200	1.5		kΩ
Mixer Peak Output Current			2.5		mA

Parameter	Conditions	Min	Typ	Max	Unit
IF FRONT END WITHOUT VGA	From MXIP, MXIN to IMXO (QMXO), ENVG = 0 V, IMXO/QMXO load = 1.5 kΩ				
Input Impedance	Measured differentially across MXIP/MXIN		200||1.5		Ω||pF
Conversion voltage Gain			10.5		dB
3 dB Output Bandwidth			75		MHz
IF Gain Flatness	F_{IF} = 380 MHZ ± 5%		0.1		dB p-p
	F_{IF} = 900 MHZ ± 5%		0.15		dB p-p
Input 1 dB Compression Point (P1dB)			−4		dBm
Third-Order Input Intercept (IIP3)	IF1 = 381 MHz, IF2 = 381.02 MHz Each tone 10 dB below P1dB from 200 Ω source		14		dBm
LO Leakage	Measured at MXIP/MXIN		−70		dBm
	Measured at IMXO, QMXO		−60		dBm
Demodulation Bandwidth	Small signal 3 dB bandwidth		75		MHz
Quadrature Phase Error	LO = 380 MHz (LOIP/LOIN 760 MHz, single-ended)	−2	±0.5	+2	Degrees
I/Q Amplitude Imbalance			0.25		dB
Noise Figure (Double Sideband)	From 200 Ω source, F_{IF} = 380 MHz		21		dB
I/Q BASEBAND AMPLIFIER	From IAIN to IOPP/IOPN and QAIN to QOPP/QOPN, R_{LOAD} = 2 kΩ, single-ended to ground				
Gain			20		dB
Bandwidth	10 pF differential load		125		MHz
Output DC Offset (Differential)	LO leakage offset corrected using 500 pF capacitor on IOFS, QOFS ($V_{IOPP} - V_{IOPN}$)	−50	±12	+50	mV
Output Common-Mode Offset	($V_{IOPP} + V_{IOPN}$)/2 − VCMO	−75	±35	+75	mV
Group Delay Flatness	0 MHz to 50 MHz		3		ns p-p
Input-Referred Noise Voltage	Frequency = 1 MHz		8		nV/√Hz
Output Swing Limit (Upper)		V_S −1			V
Output Swing Limit (Lower)				0.5	V
Peak Output Current			1		mA
Input Impedance			50||1		kΩ||pF
Input Bias Current			2		µA
RESPONSE FROM IF AND MX INPUTS TO BASEBAND AMPLIFIER OUTPUT	IMXO and QMXO connected directly to IAIN and QAIN, respectively				
Gain	From MXIP/MXIN		30.5		dB
	From IFIP/IFIN, VGIN = 0.2 V		45.5		dB
	From IFIP/IFIN, VGIN = 1.2 V		1.5		dB
CONTROL INPUT/OUTPUTS					
VCMO Input Range	V_S = 5 V	0.5	1	4	V
	V_S = 2.7 V	0.5	1	1.7	V
VREF Output Voltage		0.95	1	1.05	V
Gain Control Voltage Range	VGIN	0.2		1.2	V
Gain Slope		−55	−50	−45	dB/V
Gain Intercept	Linear extrapolation back to theoretical gain at VGIN = 0 V	55	61	67	dB
Gain Control Input Bias Current			1		µA
LO INPUTS					
LOIP Input Return Loss	LOIN ac-coupled to ground (760 MHz applied to LOIP)		−6		dB

Parameter	Conditions	Min	Typ	Max	Unit
POWER-UP CONTROL					
ENBL Threshold Low	Low = standby	0	$V_S/2$	1	V
ENBL Threshold High	High = enable	$V_S - 1$	$V_S/2$	V_S	V
Input Bias Current			2		µA
Power-Up Time	Time for final baseband amplifiers to be within 90% of final amplitude		45		µs
Power-Down Time	Time for supply current to be <10% of enabled value		700		ns
POWER SUPPLIES	VPOS1, VPOS2, VPOS3				
Voltage		2.7		5.5	V
Current (Enabled)	$V_S = 5$ V, $V_{ENBL} = 5$ V	38	48	58	mA
Current (Standby)	$V_S = 5$ V, $V_{ENBL} = 0$ V		75		µA

[1] These parameters are guaranteed but not tested in production. Limits are ±6 Σ from the mean.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage on VPOS1, VPOS2, VPOS3 Pins	5.5 V
LO Input Power	10 dBm (re: 50 Ω)
IF Input Power	18 dBm (re: 200 Ω)
Internal Power Dissipation	450 mW
θ_{JA}	68°C/W
Maximum Junction Temperature	150°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +125°C
Lead Temperature (Soldering, 60 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

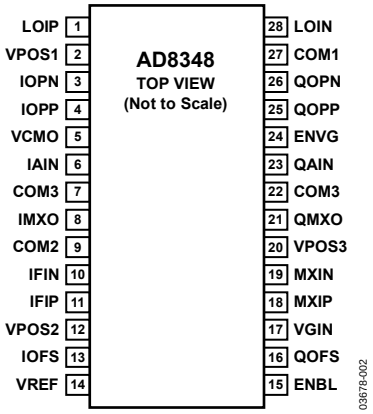


Figure 2. 28-Lead TSSOP Pin Configuration

Table 3. Pin Function Descriptions—28-Lead TSSOP

Pin No.	Mnemonic	Description	Equivalent Circuit
1, 28	LOIP, LOIN	LO Inputs. For optimum performance, these inputs should be ac-coupled and driven differentially. Differential drive from single-ended sources can be achieved via a balun. To obtain a broadband 50 Ω input impedance, connect a 60.4 Ω shunt resistor between LOIP and LOIN. Typical input drive level is equal to −10 dBm.	A
2, 12, 20	VPOS1, VPOS2, VPOS3	Positive Supply for LO, IF, and Biasing and Baseband Sections, Respectively. These pins should be decoupled with 0.1 µF and 100 pF capacitors.	
3, 4, 25, 26	IOPN, IOPP, QOPP, QOPN	I- and Q-Channel Differential Baseband Outputs. Typical output swing is equal to 2 V p-p differential. The dc common-mode voltage level on these pins is set by the voltage on VCMO.	B
5	VCMO	Baseband DC Common-Mode Voltage. The voltage applied to this pin sets the dc common-mode levels for all the baseband outputs and inputs (IMXO, QMXO, IOPP, IOPN, QOPP, QOPN, IAIN, and QAIN). This pin can be connected either to VREF or to a reference voltage from another device (typically an ADC).	C
6, 23	IAIN, QAIN	I- and Q-Channel Baseband Amplifier Inputs. The single-ended signals on these pins are referenced to VCMO and must have a dc bias equal to the dc voltage on the VCMO pin. If IMXO (QMXO) is dc-coupled to IAIN (QAIN), biasing will be provided by IMXO (QMXO). If an ac-coupled filter is placed between IMXO and IAIN, these pins can be biased from the source driving VCMO through a 1 kΩ resistor. The gain from IAIN/QAIN to the differential outputs (IOPP/IOPN and QOPP/QOPN) is 20 dB.	D
7, 22	COM3	Ground for Biasing and Baseband Sections.	
8, 21	IMXO, QMXO	I- and Q-Channel Mixer Baseband Outputs. These are low impedance (40 Ω) outputs whose bias levels are set by the voltage applied to the VCMO pin. These pins are typically connected to IAIN and QAIN, respectively, either directly or through a filter. Each output can drive a maximum current of 2.5 mA.	H
9	COM2	IF Section Ground.	
10, 11	IFIN, IFIP	IF Inputs. IFIN should be ac-coupled to ground. The single-ended IF input signal should be ac-coupled into IFIP. The nominal differential input impedance of these pins is 200 Ω. For a broadband 50 Ω input impedance, a minimum-loss L pad should be used; R_{SERIES} = 174 Ω, R_{SHUNT} = 57.6 Ω. This provides a 200 Ω source impedance to the IF input. However, the AD8348 does not necessarily require a 200 Ω source impedance, and a single shunt 66.7 Ω resistor can be placed between IFIP and IFIN.	E
13, 16	IOFS, QOFS	I- and Q-Channel Offset Nulling Inputs. DC offsets on the I-channel mixer output (IMXO) can be nulled by connecting a 0.1 µF capacitor from IOFS to ground. Driving IOFS with a fixed voltage (typically a DAC calibrated such that the offset at IOPP/IOPN is nulled) can extend the operating frequency range to include dc. The QOFS pin can likewise be used to null offsets on the Q-channel mixer output (QMXO).	F
14	VREF	Reference Voltage Output. This output voltage (1 V) is the main bias level for the device and can be used to externally bias the inputs and outputs of the baseband amplifiers. The typical maximum drive current for this output is 2 mA.	G

Pin No.	Mnemonic	Description	Equivalent Circuit
15	ENBL	Chip Enable Input. Active high. Threshold is equal to $V_S/2$.	D
17	VGIN	Gain Control Input. The voltage on this pin controls the gain on the IF VGA. The gain control voltage range is from 0.2 V to 1.2 V and corresponds to a conversion gain range from +25.5 dB to −18.5 dB. This is the gain to the output of the mixers (that is, IMXO and QMXO). There is an additional 20 dB of fixed gain in the final baseband amplifiers (IAIN to IOPP/IOPN and QAIN to QOPP/QOPN). Note that the gain control function has a negative sense (that is, increasing voltage decreases gain).	D
18, 19	MXIP, MXIN	Auxiliary Mixer Inputs. If ENVG is low, the IFIP and IFIN inputs are disabled and MXIP and MXIN are enabled, allowing the VGA to be bypassed. The auxiliary mixer inputs are fully differential inputs that should be ac-coupled to the signal source.	I
24	ENVG	Active High VGA Enable. When ENVG is high, IFIP and IFIN inputs are enabled and MXIP and MXIN inputs are disabled. When ENVG is low, MXIP and MXIN inputs are enabled and IFIP and IFIN inputs are disabled.	D
27	COM1	LO Section Ground.	

EQUIVALENT CIRCUITS

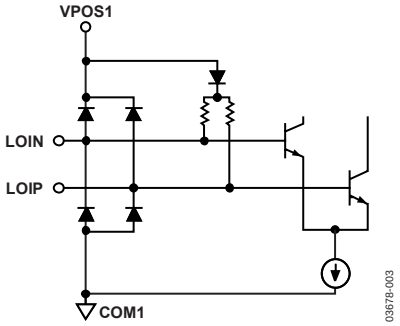


Figure 3. Circuit A

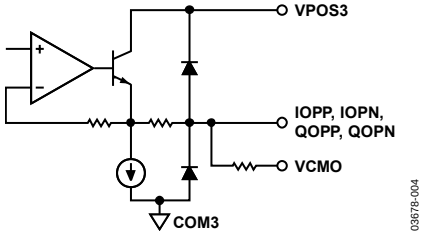


Figure 4. Circuit B

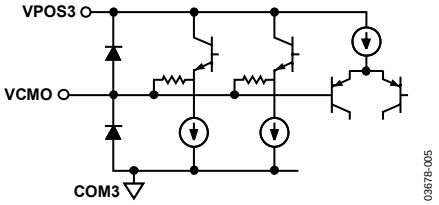


Figure 5. Circuit C

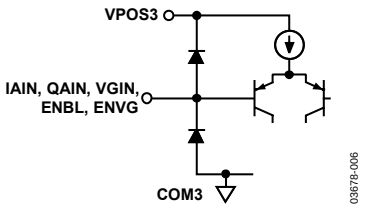


Figure 6. Circuit D

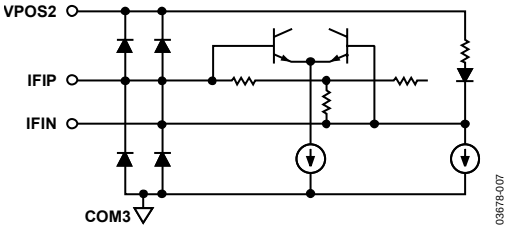


Figure 7. Circuit E

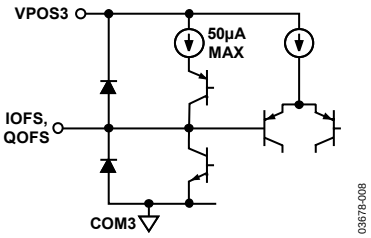


Figure 8. Circuit F

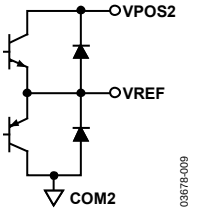


Figure 9. Circuit G

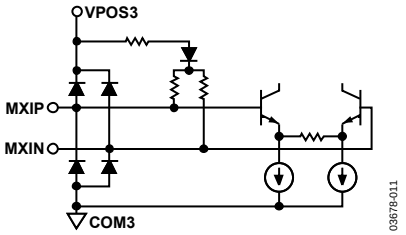


Figure 11. Circuit I

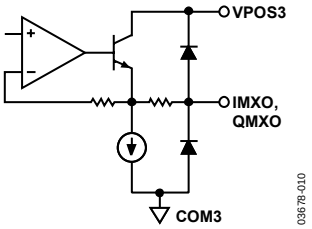


Figure 10. Circuit H

TYPICAL PERFORMANCE CHARACTERISTICS

VGA AND DEMODULATOR

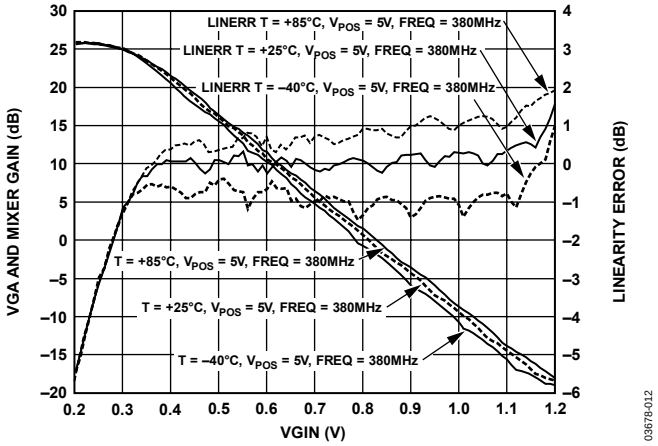


Figure 12. Mixer Gain and Linearity Error vs. VGIN, V_{POS} = 5 V, F_{IF} = 380 MHz, F_{BB} = 1 MHz, Temperature = –40°C, +25°C, +85°C

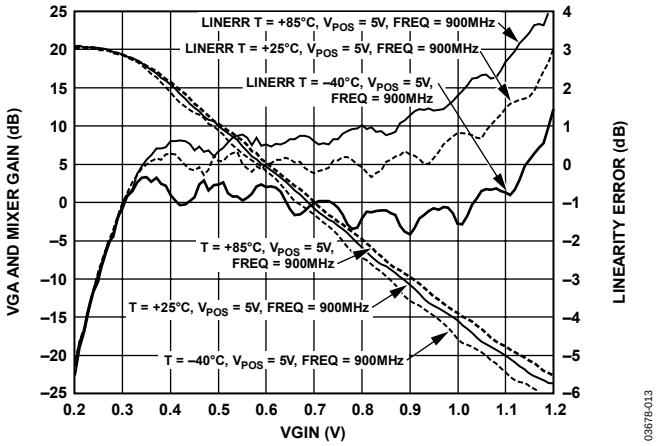


Figure 13. Mixer Gain and Linearity Error vs. VGIN, V_{POS} = 5 V, F_{IF} = 900 MHz, F_{BB} = 1 MHz, Temperature = –40°C, +25°C, +85°C

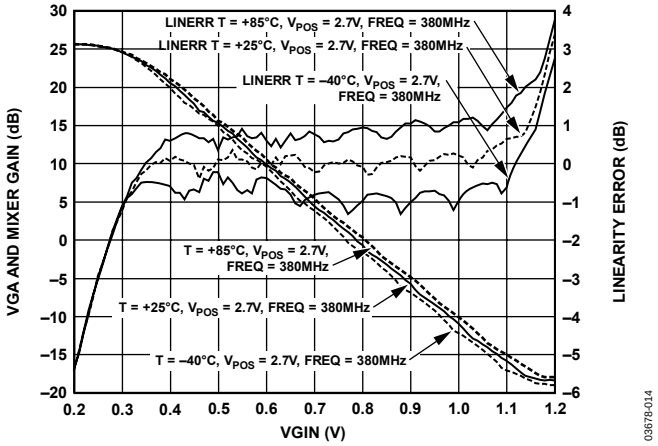


Figure 14. Mixer Gain and Linearity Error vs. VGIN, V_{POS} = 2.7 V, F_{IF} = 380 MHz, F_{BB} = 1 MHz, Temperature = –40°C, +25°C, +85°C

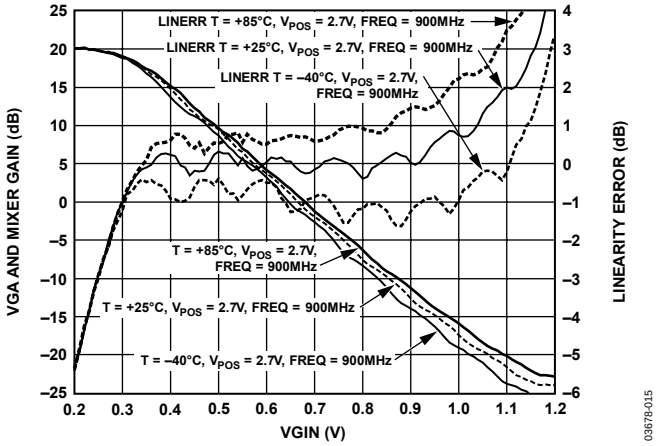


Figure 15. Mixer Gain and Linearity Error vs. VGIN, V_{POS} = 2.7 V, F_{IF} = 900 MHz, F_{BB} = 1 MHz, Temperature = –40°C, +25°C, +85°C

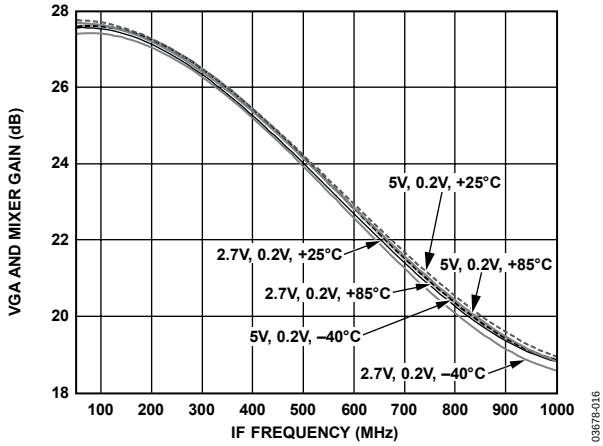


Figure 16. Gain vs. F_{IF}, VGIN = 0.2 V, F_{BB} = 1 MHz, Temperature = –40°C, +25°C, +85°C

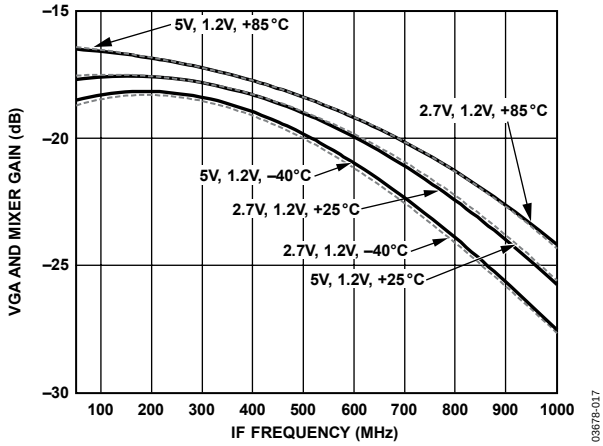


Figure 17. Gain vs. F_{IF}, VGIN = 1.2 V, F_{BB} = 1 MHz, Temperature = –40°C, +25°C, +85°C

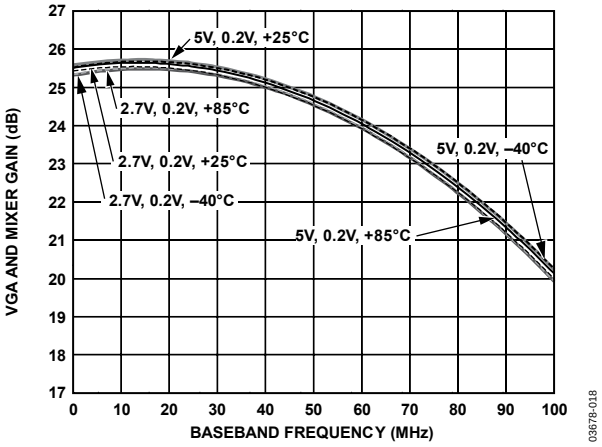


Figure 18. Gain vs. F_{BB}, VGIN = 0.2 V, F_{IF} = 380 MHz, V_{POS} = 2.7 V, 5 V, Temperature = −40°C, +25°C, +85°C

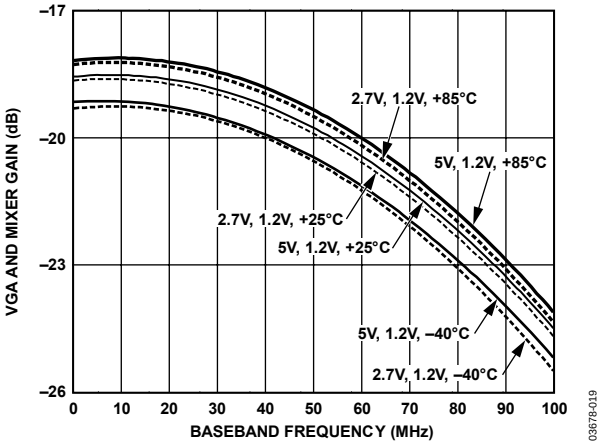


Figure 19. Gain vs. F_{BB}, VGIN = 1.2 V, F_{IF} = 380 MHz, V_{POS} = 2.7 V, 5 V, Temperature = −40°C, +25°C, +85°C

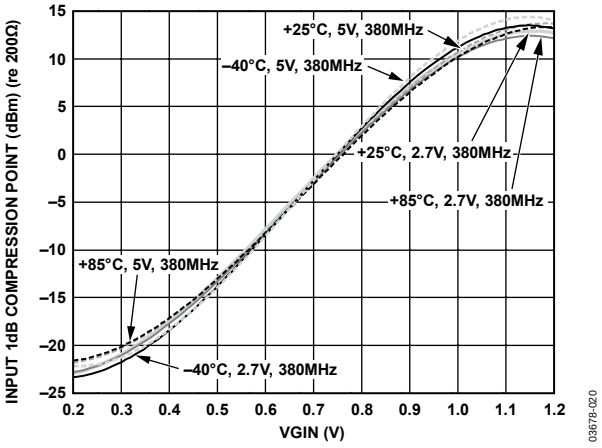


Figure 20. Input 1 dB Compression Point (IP1dB) vs. VGIN, F_{IF} = 380 MHz, F_{BB} = 1 MHz, V_{POS} = 2.7 V, 5 V, Temperature = −40°C, +25°C, +85°C

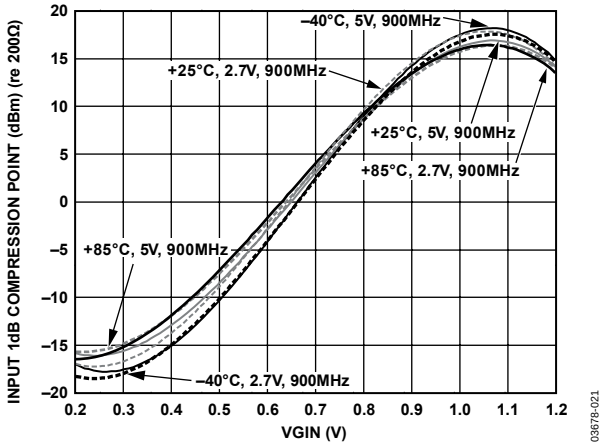


Figure 21. Input 1 dB Compression Point (IP1dB) vs. VGIN, F_{IF} = 900 MHz, F_{BB} = 1 MHz, V_{POS} = 2.7 V, 5 V, Temperature = −40°C, +25°C, +85°C

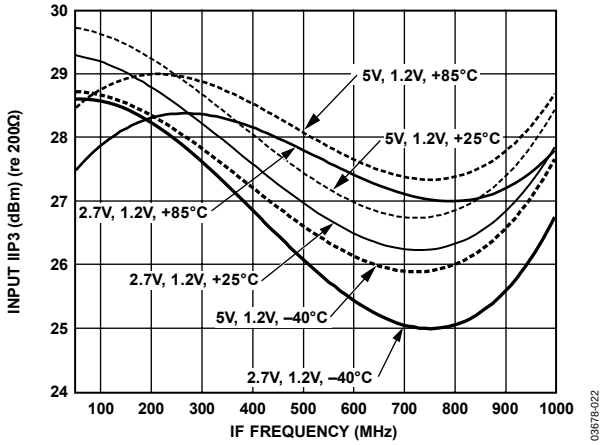


Figure 22. IIP3 vs. F_{IF}, VGIN = 1.2 V, F_{BB} = 1 MHz, V_{POS} = 2.7 V, 5 V, Temperature = −40°C, +25°C, +85°C, Tone Spacing = 20 kHz

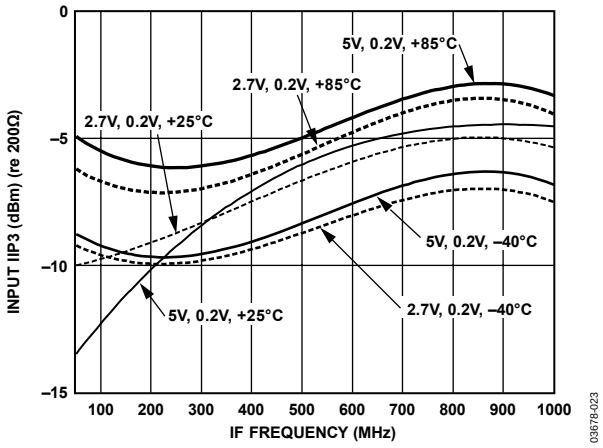


Figure 23. IIP3 vs. F_{IF}, VGIN = 0.2 V, F_{BB} = 1 MHz, V_{POS} = 2.7 V, 5 V, Temperature = −40°C, +25°C, +85°C

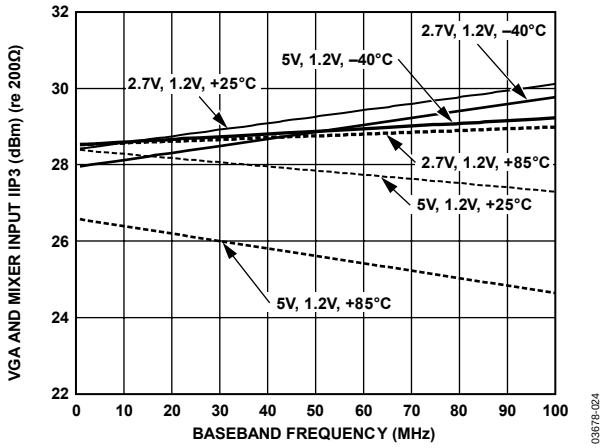


Figure 24. IIP3 vs. F_{BB}, VGIN = 1.2 V, F_{IF} = 380 MHz, V_{POS} = 2.7 V, 5 V, Temperature = –40°C, +25°C, +85°C

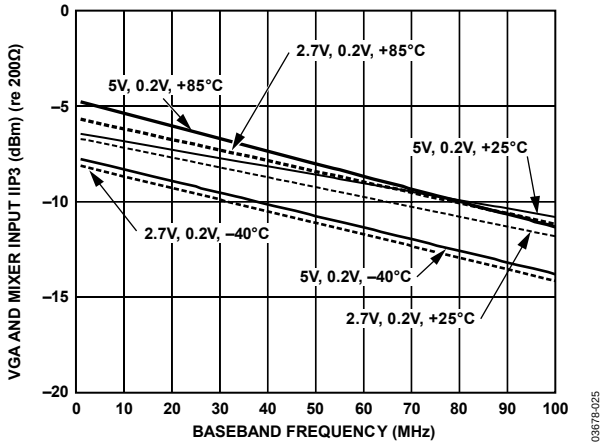


Figure 25. IIP3 vs. F_{BB}, VGIN = 0.2 V, F_{IF} = 380 MHz, V_{POS} = 2.7 V, 5 V, Temperature = –40°C, +25°C, +85°C

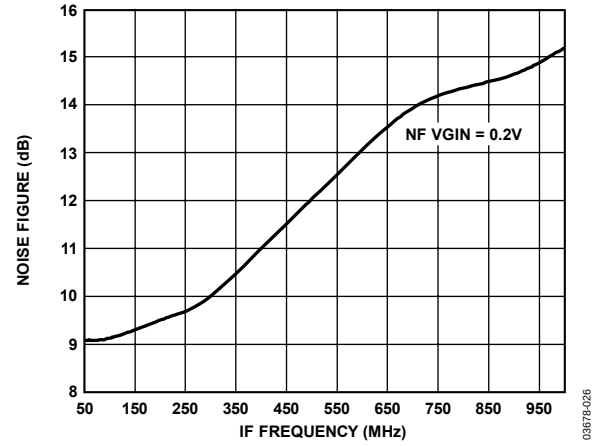


Figure 26. Noise Figure vs. F_{IF}, T = 25°C, VGIN = 0.2 V, F_{BB} = 1 MHz

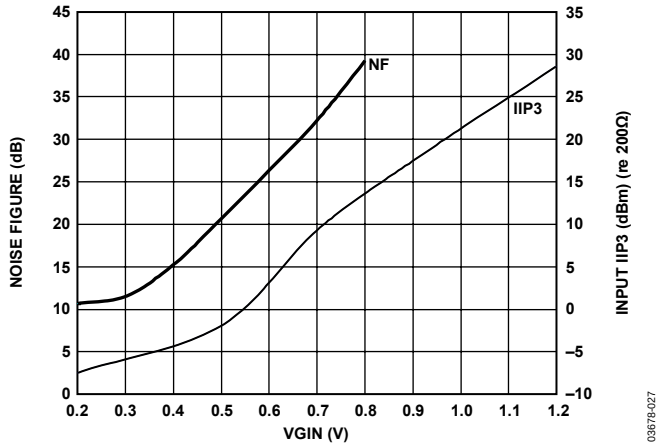


Figure 27. Noise Figure and IIP3 vs. VGIN, Temperature = 25°C, F_{IF} = 380 MHz, F_{BB} = 1 MHz, V_{POS} = 2.7 V

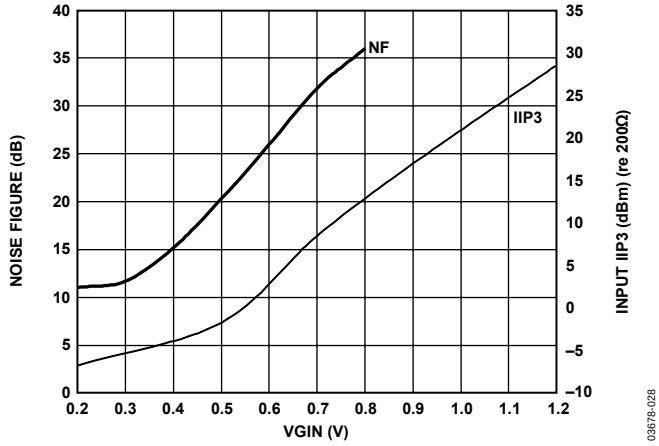


Figure 28. Noise Figure and IIP3 vs. VGIN, Temperature = 25°C, F_{IF} = 380 MHz, F_{BB} = 1 MHz, V_{POS} = 5 V

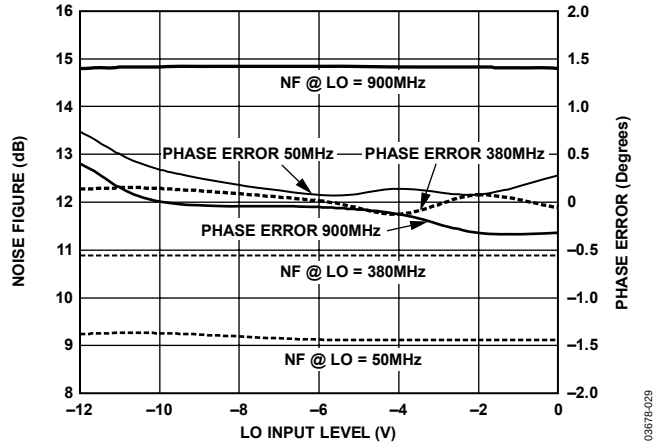


Figure 29. Noise Figure and Quadrature Phase Error IMXO/QMXO vs. LO Input Level, Temperature = 25°C, VGIN = 0.2 V, V_{POS} = 5 V for F_{IF} = 50 MHz, 380 MHz, and 900 MHz

DEMODULATOR USING MXIP AND MXIN

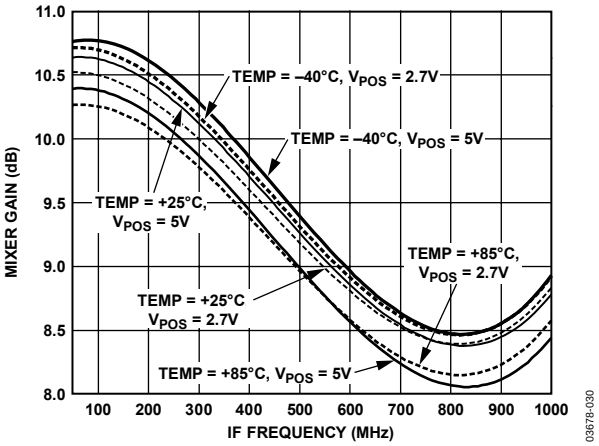


Figure 30. Mixer Gain vs. F_{IF}, V_{POS} = 2.7 V, 5 V, F_{BB} = 1 MHz, Temperature = −40°C, +25°C, +85°C

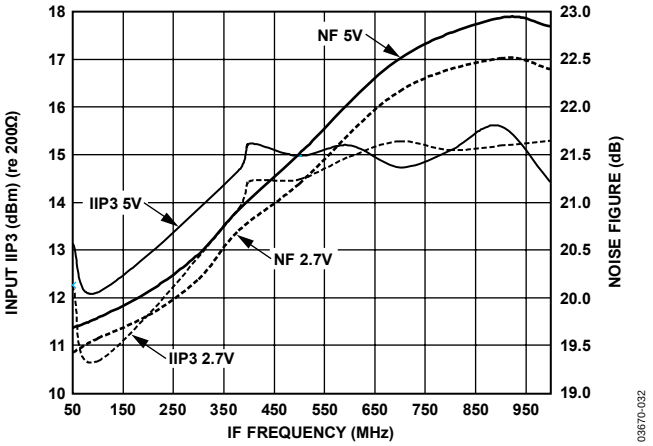


Figure 32. IIP3 and Noise Figure vs. F_{IF}, V_{POS} = 2.7 V, 5 V, Temperature = 25°C

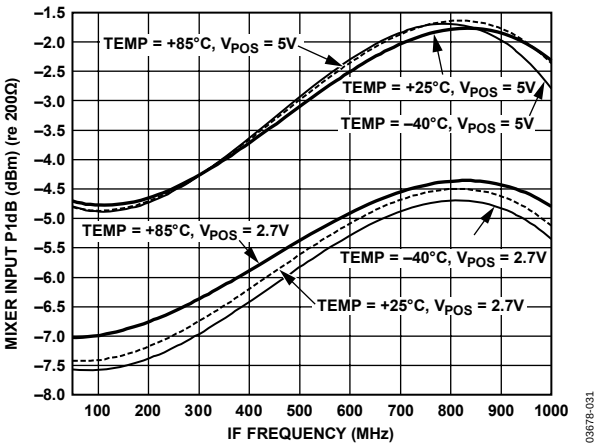


Figure 31. Input 1 dB Compression Point vs. F_{IF}, F_{BB} = 1 MHz, V_{POS} = 2.7 V, 5 V, Temperature = −40°C, +25°C, +85°C

FINAL BASEBAND AMPLIFIERS

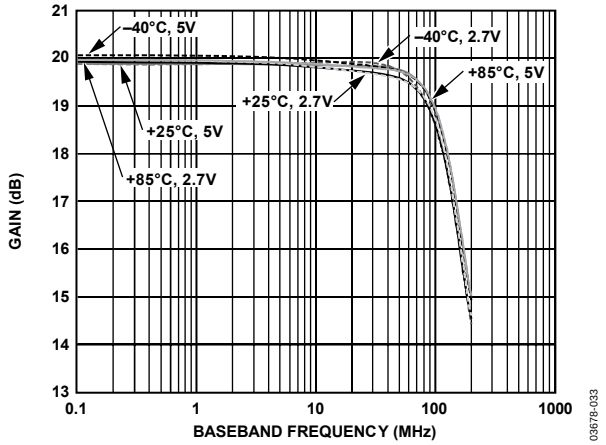


Figure 33. Gain vs. F_{BB}, V_{VCMO} = VREF = 1 V, V_{POS} = 2.7 V, 5 V, Temperature = −40°C, +25°C, +85°C

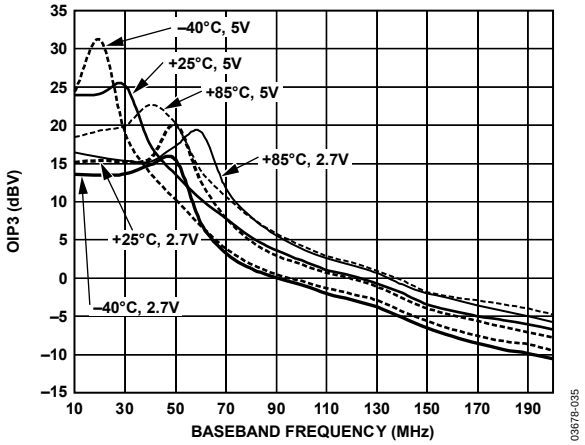


Figure 35. OIP3 vs. F_{BB}, V_{VCMO} = VREF = 1 V, V_{POS} = 2.7 V, 5 V, Temperature = −40°C, +25°C, +85°C

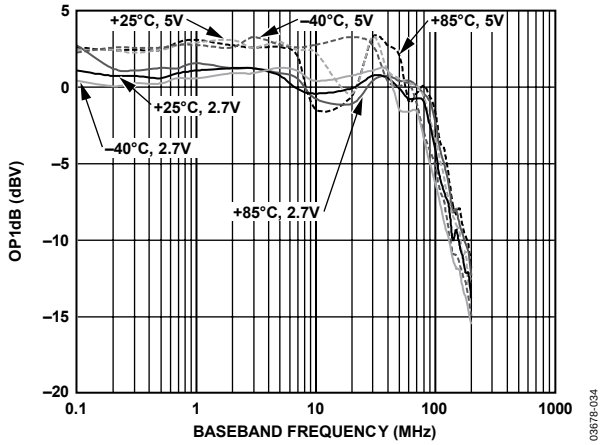


Figure 34. OP1dB Compression vs. F_{BB}, V_{VCMO} = VREF = 1 V, V_{POS} = 2.7 V, 5 V, Temperature = −40°C, +25°C, +85°C

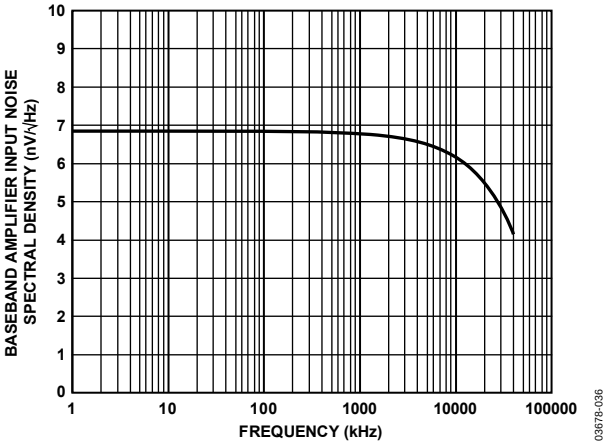


Figure 36. Noise Spectral Density

VGA/DEMODULATOR AND BASEBAND AMPLIFIER

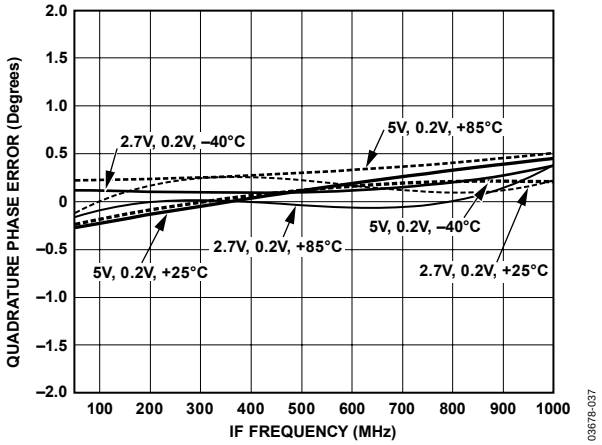


Figure 37. Quadrature Phase Error vs. F_{IF}, VGIN = 0.7 V, V_{POS} = 2.7 V, 5 V, Temperature = −40°C, +25°C, +85°C

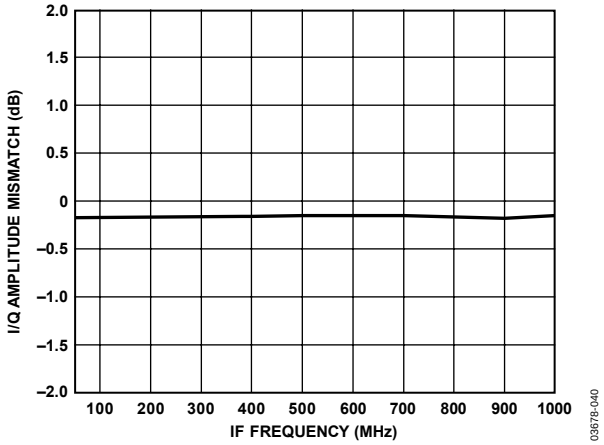


Figure 40. I/Q Amplitude Imbalance vs. F_{IF}, Temperature = 25°C, V_{POS} = 5 V

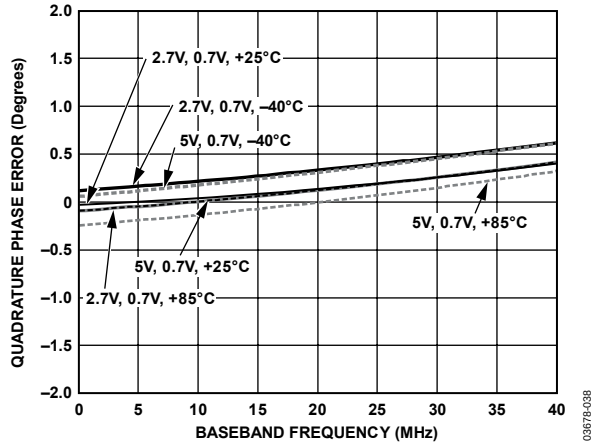


Figure 38. Quadrature Phase Error vs. F_{BB}, VGIN = 0.7 V, V_{POS} = 2.7 V, 5 V, Temperature = −40°C, +25°C, +85°C, F_{IF} = 380 MHz

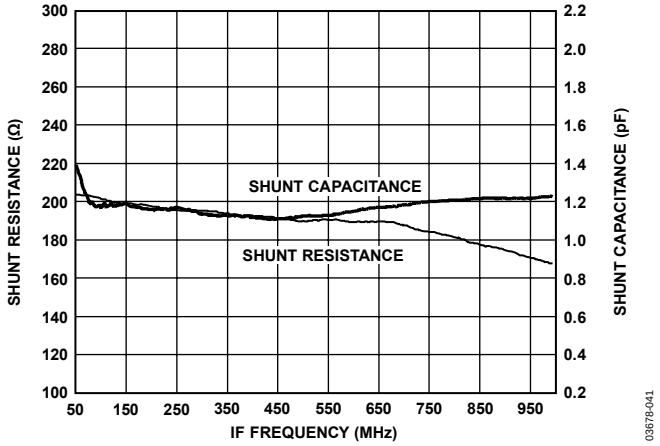


Figure 41. Input Impedance of IF Input vs. F_{IF}, VGIN = 0.7 V, V_{POS} = 5 V

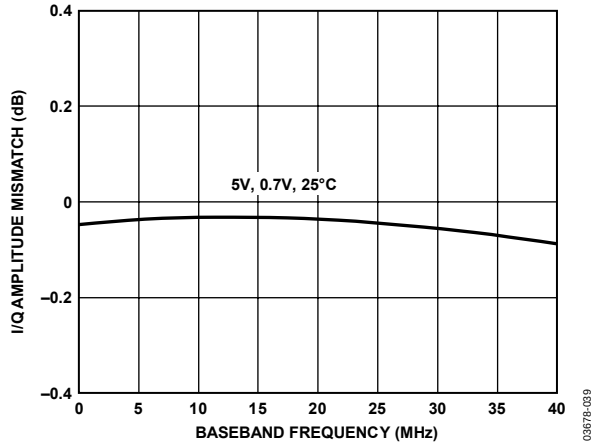


Figure 39. I/Q Amplitude Imbalance vs. F_{BB}, Temperature = 25°C, V_{POS} = 5 V

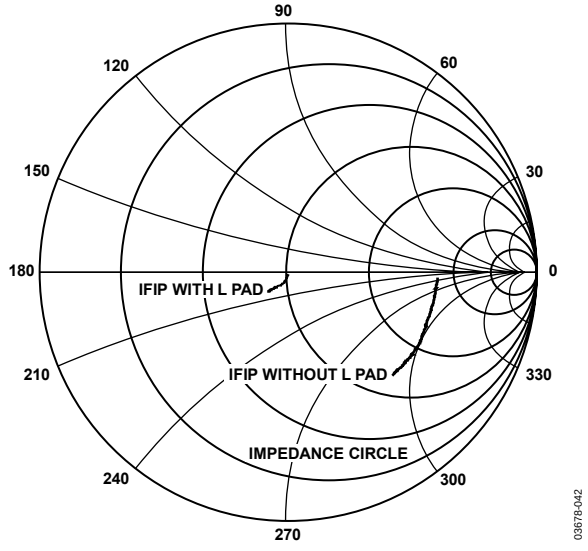


Figure 42. S11 of IF Input vs. F_{IF}, F_{IF} = 50 MHz to 1 GHz, VGIN = 0.7 V, V_{POS} = 5 V (with L Pad, with No Pad, Normalized to 50 Ω)

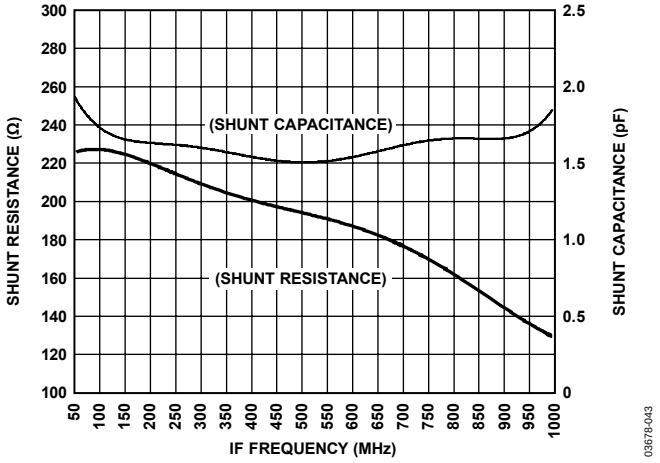


Figure 43. Input Impedance of Mixer Input vs. F_{IF}, VGIN = 0.7 V, V_{POS} = 5 V

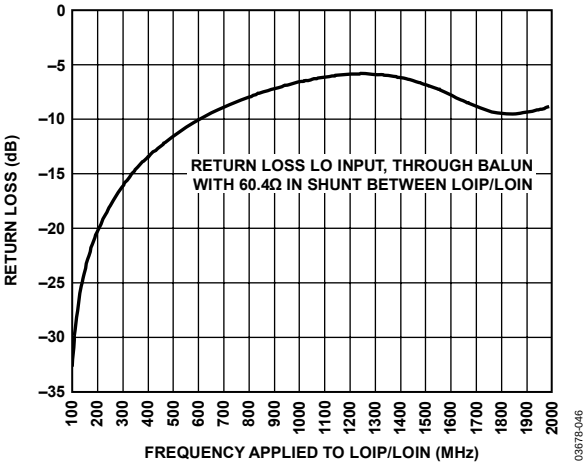


Figure 46. Return Loss of LO Input vs. External LO Frequency Through Balun, with Termination Resistor

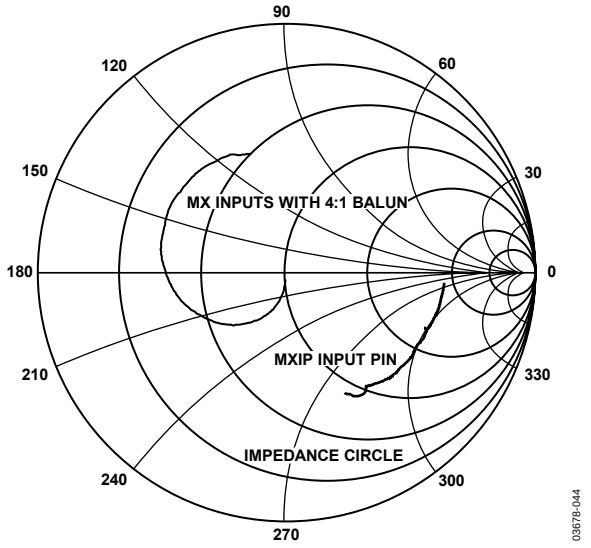


Figure 44. S11 of Mixer Input vs. F_{IF}, F_{IF} = 50 MHz to 1 GHz, VGIN = 0.7 V, V_{POS} = 5 V (With and Without Balun)

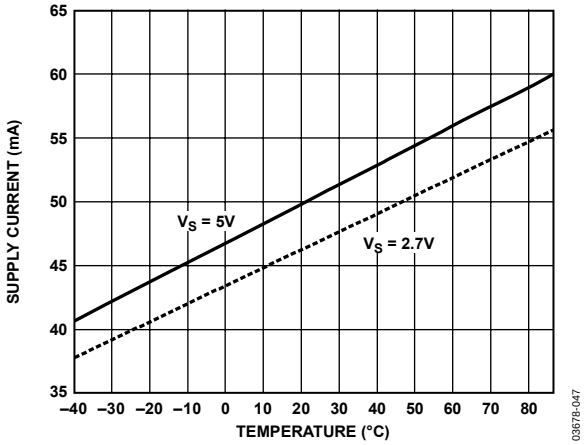


Figure 47. Supply Current vs. Temperature

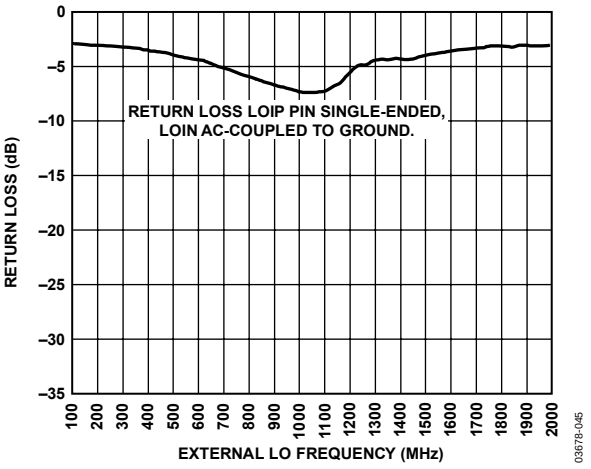


Figure 45. Return Loss of LOIP Input vs. External LO Frequency

THEORY OF OPERATION

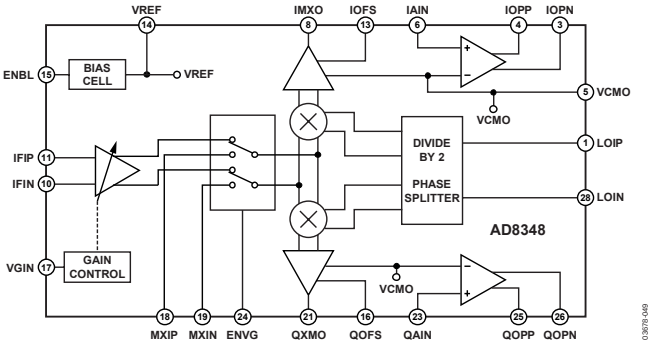


Figure 48. Functional Block Diagram

VGA

The VGA is implemented using the patented X-AMP architecture. The single-ended IF signal is attenuated in eight discrete 6 dB steps by a passive R-2R ladder. Each discrete attenuated version of the IF signal is applied to the input of a transconductance stage. The current outputs of all transconductance stages are summed together and drive a resistive load at the output of the VGA. Gain control is achieved by smoothly turning on and off the relevant transconductance stages with a temperature-compensated interpolation circuit. This scheme allows the gain to continuously vary over a 44 dB range with linear-in-decibel gain control. This configuration also keeps the relative dynamic range constant (for example, IIP3 − NF in dB) over the gain setting; however, the absolute intermodulation intercepts and noise figure vary directly with gain. The analog voltage VGIN sets the gain. VGIN = 0.2 V is the maximum gain setting, and VGIN = 1.2 V is the minimum voltage gain setting.

DOWNCONVERSION MIXERS

The output of the VGA drives two (I and Q) double-balanced Gilbert cell downconversion mixers. Alternatively, driving the ENVG pin low can disable the VGA, and the mixers can be externally driven directly via the MXIP and MXIN ports. At the input of the mixer, a degenerated differential pair performs linear voltage-to-current conversions. The differential output current feeds into the mixer core where it is downconverted by the mixing action of the Gilbert cell. The phase splitter provides quadrature LO signals that drive the LO ports of the in-phase and quadrature mixers.

Buffers at the output of each mixer drive the IMXO and QMXO pins. These linear, low output impedance buffers drive 40 Ω, temperature-stable, passive resistors in series with each output pin (IMXO and QMXO). This 40 Ω should be considered when calculating the reverse termination if an external filter is inserted between IMXO (QMXO) and IAIN (QAIN). The VCMO pin sets the dc output level of the buffer. This can be set externally or connected to the on-chip 1.0 V reference, VREF.

PHASE SPLITTER

Quadrature generation is achieved using a divide-by-2 frequency divider. Unlike a polyphase filter that achieves quadrature over a limited frequency range, the divide-by-2 approach maintains quadrature over a broad frequency range and does not attenuate the LO. The user, however, must provide an external signal XLO that is twice the frequency of the desired LO frequency. XLO drives the clock inputs of two flip-flops that divide down the frequency by a factor of 2. The outputs of the two flip-flops are one-half period of XLO out of phase. Equivalently, the outputs are one-quarter period (90°) of the desired LO frequency out of phase. Because the transitions on XLO define the phase difference at the outputs, deviation from 50% duty cycle translates directly to quadrature phase errors.

If the user generates XLO from a 1× frequency (f_{REF}) and a frequency-doubling circuit (XLO = 2 × f_{REF}), fundamentally there is a 180° phase uncertainty between f_{REF} and the AD8348 internal quadrature LO. The phase relationship between I and Q LO, however, is always 90°.

I/Q BASEBAND AMPLIFIERS

Two (I and Q) fixed gain (20 dB), single-ended-to-differential amplifiers are provided to amplify the demodulated signal after off-chip filtering. The amplifiers use voltage feedback to linearize the gain over the demodulation bandwidth. These amplifiers can be used to maximize the dynamic range at the input of an ADC following the AD8348.

The input to the baseband amplifiers, IAIN (QAIN), feeds into the base of a bipolar transistor with an input impedance of roughly 50 kΩ. The baseband amplifiers sense the single-ended difference between IAIN (QAIN) and VCMO. IAIN (QAIN) can be dc biased by terminating it with a shunt resistor to VCMO, such as when an external filter is inserted between IMXO (QMXO) and IAIN (QAIN). Alternatively, any dc connection to IMXO (QXMO) can provide appropriate bias via the offset-nulling loop.

ENABLE

A master biasing cell that can be disabled using the ENBL pin controls the biasing for the chip. If the ENBL pin is held low, the entire chip powers down to a low power sleep mode, typically consuming 75 μA at 5 V.

BASEBAND OFFSET CANCELLATION

A low output current integrator senses the output voltage offset at IOPP and IOPN (QOPP and QOPN) and injects a nulling current into the signal path. The integration time constant of the offset-nulling loop is set by Capacitor COFS from IOFS (QOFS) to

VCMO. This forms a high-pass response for the baseband signal path with a lower 3 dB frequency of

$$f_{PASS} = \frac{1}{2\pi \times 2650\ \Omega\ \times COFS}$$

Alternatively, the user can externally adjust the dc offset by driving IOFS (QOFS) with a digital-to-analog converter or other voltage source. In this case, the baseband circuit operates all the way down to dc (f_{PASS} = 0 Hz). The integrator output current is only 50 μA and can be easily overridden with an external voltage source. The nominal voltage level applied to IOFS (QOFS) to produce a 0 V differential offset at the baseband outputs is 900 mV.

The IOFS (QOFS) pin must be connected to either a bypass capacitor (>0.1 μF) or an external voltage source to prevent the feedback loop from oscillating.

The feedback loop will be broken at dc if an ac-coupled baseband filter is placed between the mixer outputs and the baseband amplifier inputs. If an ac-coupled filter is implemented, the user must handle the offset compensation via some external means.

APPLICATIONS

BASIC CONNECTIONS

Figure 49 shows the basic connections schematic for the AD8348.

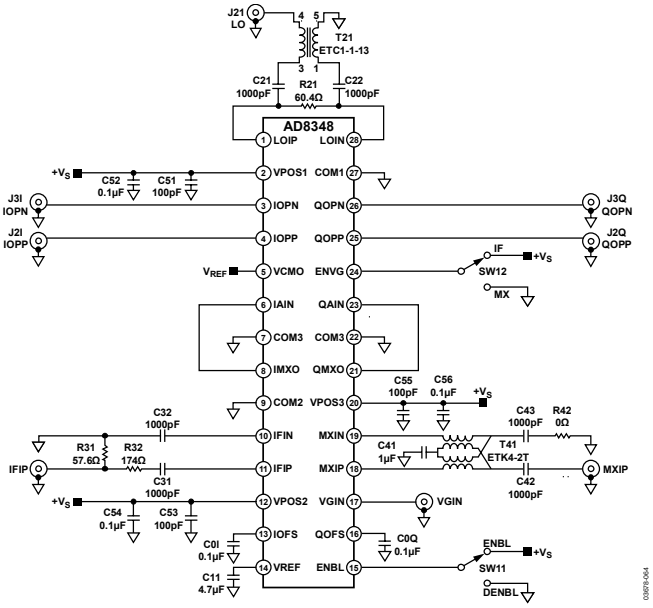


Figure 49. Basic Connections Schematic

POWER SUPPLY

The voltage supply for the AD8348, between 2.7 V and 5 V, should be provided to the +VPOSx pins, and ground should be connected to the COMx pins. Each supply pin should be decoupled separately using two capacitors whose recommended values are 100 pF and 0.1 µF (values close to these can also be used).

DEVICE ENABLE

To enable the device, the ENBL pin should be driven to V_S. Grounding the ENBL pin disables the device.

VGA ENABLE

Driving the voltage on the ENVG pin to V_S enables the VGA. In this mode, the MX inputs are disabled and the IF inputs are used. Grounding the ENVG pin disables the VGA and the IF inputs. When the VGA is disabled, the MX inputs should be used.

GAIN CONTROL

When the VGA is enabled, the voltage applied to the VGIN pin sets the gain. The gain control voltage range is between 0.2 V and 1.2 V. This corresponds to a gain range between +25.5 dB and −18.5 dB.

LO INPUTS

For optimum performance, the local oscillator port should be driven differentially through a balun. The recommended balun is M/A-COM ETC1-1-13. The LO inputs to the device should be ac-coupled, unless an ac-coupled transformer is being used. For a broadband match to a 50 Ω source, a 60.4 Ω resistor should be placed between the LOIP and LION pins.

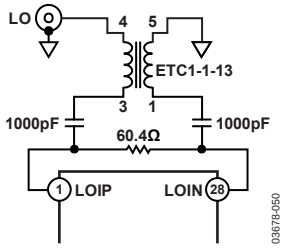


Figure 50. Differential LO Drive with Balun

Alternatively, the LO port can be driven from a single-ended source without a balun (Figure 51). The LO signal is ac-coupled directly into the LOIP pin via an ac-coupling capacitor, and the LOIN pin is ac-coupled to ground. Driving the LO port from a single-ended source results in an increase in both quadrature phase error and LO leakage.

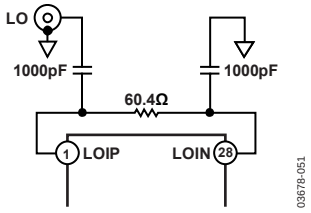


Figure 51. Single-Ended LO Drive

The recommended LO drive level is between −12 dBm and 0 dBm. The LO frequency at the input to the device should be twice that of the desired LO frequency at the mixer core. The applied LO frequency range is between 100 MHz and 2 GHz.

IF INPUTS

The IF inputs have an input impedance of 200 Ω. A broadband 50 Ω match can be presented to the driving source through the use of a minimum-loss L pad. This minimum-loss pad introduces an 11.46 dB loss in the input path and must be taken into account when calculating metrics such as gain and noise figure. Figure 42 shows the S11 of the IF input with and without the L pad.

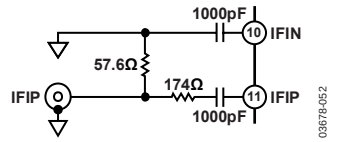


Figure 52. Minimum-Loss L Pad for 50 Ω IF Input

MX INPUTS

The mixer inputs, MXIP and MXIN, have a nominal impedance of 200 Ω and should be driven differentially. When driven from a differential source, the input should be ac-coupled to the source via capacitors, as shown in Figure 53.

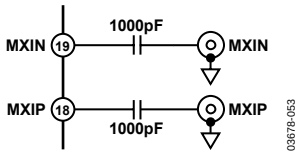


Figure 53. Driving the MX Inputs from a Differential Source

If the MX inputs are to be driven from a single-ended 50 Ω source, a 4:1 balun can be used to transform the 200 Ω impedance of the inputs to 50 Ω while performing the required single-ended-to-differential conversion. The recommended transformer is the M/A-COM ETK4-2T.

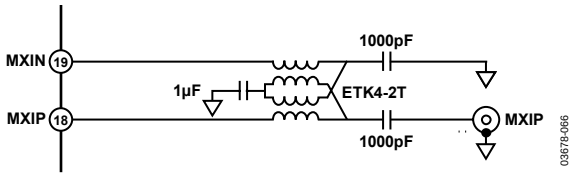


Figure 54. Driving the MX Inputs from a Single-Ended 50 Ω Source

BASEBAND OUTPUTS

The baseband amplifier outputs, IOPP, IOPN, QOPP, and QOPN, should be presented with loads of at least 2 kΩ (single-ended to ground). They are not designed to drive 50 Ω loads directly. The typical swing for these outputs is 2 V p-p differential (1 V p-p single-ended), but larger swings are possible as long as care is taken to ensure that the signals remain within the lower limit of 0.5 V and the upper limit of V_S – 1 V of the output swing. To achieve a larger swing, it is necessary to adjust the common-mode bias of the baseband output signals. Increasing the swing can have the benefit of improving the signal-to-noise ratio of the baseband amplifier output.

When connecting the baseband outputs to other devices, care should be taken to ensure that the outputs are not capacitively loaded by approximately 20 pF or more. Such loads could potentially overload the output or induce oscillations. The effect of capacitive loading on the baseband amplifier outputs can be mitigated by inserting series resistors of approximately 200 Ω.

OUTPUT DC BIAS LEVEL

The dc bias of the mixer outputs and the baseband amplifier inputs and outputs is determined by the voltage that is driven onto the VCMO pin. The range of this voltage is typically between 500 mV and 4 V when operating with a 5 V supply.

To achieve maximum voltage swing from the baseband amplifiers, VCMO should be driven at 2.25 V; this allows a swing of up to 7 V p-p differential (3.5 V p-p single-ended).

INTERFACING TO DETECTOR FOR AGC OPERATION

The AD8348 can be interfaced with a detector such as the AD8362 rms-to-dc converter to provide an automatic signal-leveling function for the baseband outputs.

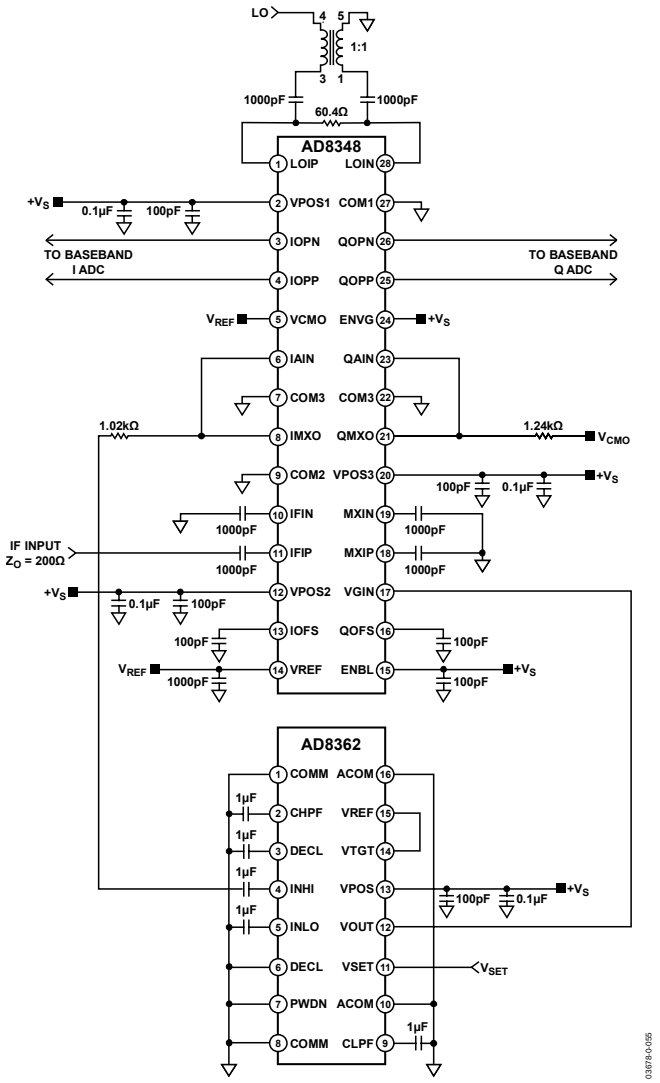


Figure 55. AD8362 Configuration for AGC Operation

Assuming the I and Q channels have the same rms power, the mixer output (or the output of the baseband filter) of one channel can be used as the input of the AD8362. The AD8362 should be operated in a region where its linearity error is small. Also, a voltage divider should be implemented with an external resistor in series with the 200 Ω input impedance of the AD8362 input. This attenuates the AD8348 mixer output so that the AD8362 input is not overdriven. The size of the resistor between the mixer output and the AD8362 input should be chosen so that the peak signal level at the input of the AD8362 is about 10 dB less than the approximately 10 dBm maximum of the AD8362 dynamic range.

The other side of the AD8348 baseband output should be loaded with a resistance equal to the series resistance of the attenuating resistor in series with the AD8362's 200 Ω input impedance. This resistor should be tied to the source driving VCMO so that there is no dc drawn from the mixer output.

The level of the mixer output (or the output of the baseband filter) can then be set by varying the setpoint voltage fed to Pin 11 (VSET) of the AD8362.

Care should be taken to ensure that blockers—unwanted signals in the band of interest that are demodulated along with the desired signal—do not dominate the rms power of the AD8362 input. This can cause an undesired reduction in the level of the mixer output. To overcome this, baseband filtering can be implemented to filter out undesired signals before the signal is presented to the AD8362.

Figure 56 shows the effectiveness of the AGC loop in maintaining a baseband amplifier output amplitude with less than 0.5 dB of amplitude error over an IF input range of 40 dB while demodulating a QPSK-modulated signal at 380 MHz. The AD8362 is insensitive to crest factor variations and therefore provides similar performance regardless of the modulation of the incoming signal.

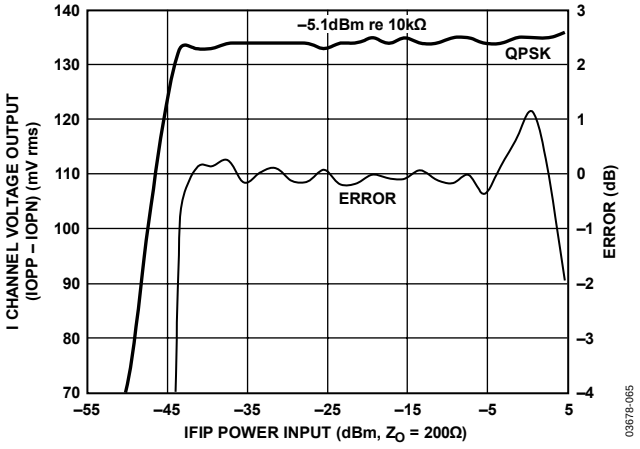


Figure 56. AD8348 Baseband Amplifier Output vs. IF Input Power with AD8362 AGC Loop

BASEBAND FILTERS

Baseband low-pass or band-pass filtering can be conveniently performed between the mixer outputs (IMXO and QMXO) and the input to the baseband amplifiers. Consideration should be given to the output impedance of the mixers (40 Ω).

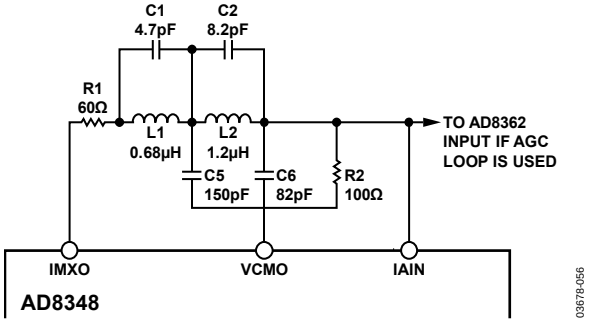


Figure 57. Baseband Filter Schematic

Figure 57 shows the schematic for a 100 Ω, fourth-order elliptic low-pass filter with a 3 dB cutoff frequency of 20 MHz. Source and load impedances of approximately 100 Ω ensure that the filter sees a matched source and load. This also ensures that the mixer output is driving an overall load of 200 Ω. Note that the shunt termination resistor is tied to the source driving VCMO and not to ground. This ensures that the input to the baseband amplifier is biased to the proper reference level. VCMO is not an output pin and must be biased by a low impedance source.

The frequency response and group delay of this filter are shown in Figure 58 and Figure 59.

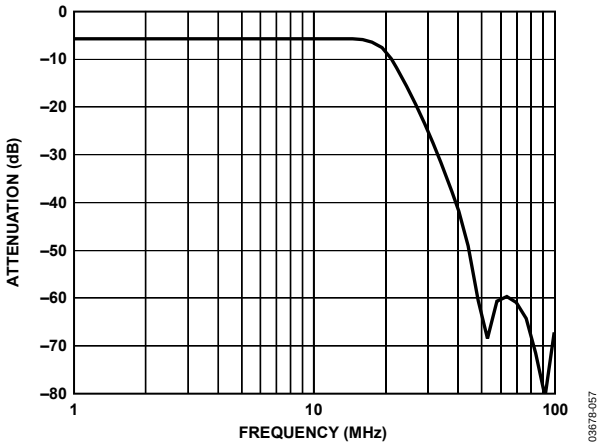


Figure 58. Baseband Filter Response

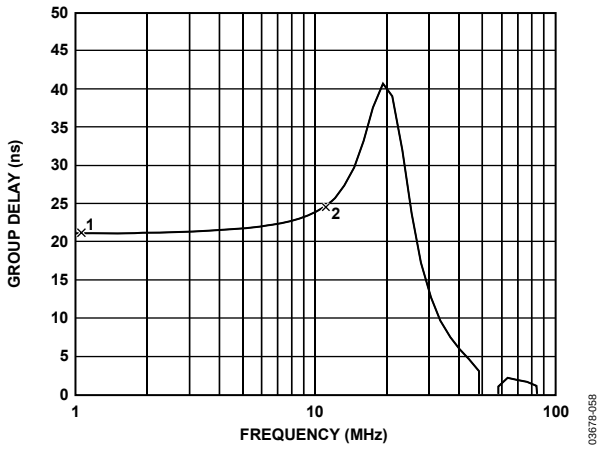


Figure 59. Baseband Filter Group Delay

LO GENERATION

Analog Devices has a line of PLLs that can be used for generating the LO signal. Table 4 lists the PLLs and their maximum frequency and phase noise performance.

Table 4. ADI PLL Selection Table

ADI Model	Frequency F_{IN} (MHz)	@ 1 kHz ΦN dBc/Hz, 200 kHz PFD
ADF4001BRU	165	−99
ADF4001BCP	165	−99
ADF4110BRU	550	−91
ADF4110BCP	550	−91
ADF4111BRU	1200	−78
ADF4111BCP	1200	−78
ADF4112BRU	3000	−86
ADF4112BCP	3000	−86
ADF4116BRU	550	−89
ADF4117BRU	1200	−87
ADF4118BRU	3000	−90

ADI also offers the ADF4360 fully integrated synthesizer and VCO on a single chip that offers differential outputs for driving the local oscillator input of the AD8348. This means that the user can eliminate the use of a balun for single-ended-to-differential conversions. The ADF4360 comes as a family of chips with six operating frequency ranges. One can be chosen depending on the local oscillator frequency required. Table 5 shows the options available.

Table 5. ADF4360 Family Operating Frequencies

ADI Model	Output Frequency Range (MHz)
ADF4360-1	2150 to 2450
ADF4360-2	1800 to 2150
ADF4360-3	1550 to 1950
ADF4360-4	1400 to 1800
ADF4360-5	1150 to 1400
ADF4360-6	1000 to 1250
ADF4360-7	Lower frequencies set by external L

EVALUATION BOARD

Figure 60 shows the schematic for the AD8348 evaluation board. Note that uninstalled components are indicated with the OPEN designation. The board is powered by a single supply in the range of 2.7 V to 5.5 V. Table 6 details the various configuration options of the evaluation board. Table 7 shows the various jumper configurations for operating the evaluation board with different signal paths.

Power to operate the board can be fed to a single V_S test point located near the LO input port at the top of the evaluation board. A GND test point is conveniently provided next to the V_S test point for the return path.

The device is enabled by moving Switch SW11 (at the bottom left of the evaluation board) to the ENBL position. The device is disabled by moving SW11 to the DENBL position. If desired, the device can be enabled and disabled from an external source that can be fed into the ENBL SMA connector or the VENB test point, in which case SW11 should be placed in the DENBL position.

The IF and MX inputs are selected via SW12. The switch should be moved in the direction of the desired input.

Gain Control

For convenience, a potentiometer, R15, is provided to allow for changes in gain without the need for an additional dc voltage source. To use the potentiometer, the SW13 switch must be set to the POT position. Alternatively, an external voltage applied to either the test point or SMA connector labeled VGIN can set the gain. SW13 must be set to the EXT position when an external gain control voltage is used.

LO Input

The local oscillator signal should be fed to the SMA Connector J21. This port is terminated in 50 Ω. The acceptable LO power input range is from −12 dBm to 0 dBm and must be at a frequency double that of the IF/MX frequency. Remember that the AD8348 uses a 2:1 frequency divider in the LO path to generate the internally required quadrature-phase-related LO signals.

IF Input

The IF input should be fed into the SMA connector IFIP. The VGA must be enabled when this port is used (SW12 in the IF position). When this IF input is chosen, the signal path includes a minimum-loss attenuator to transform a 50 Ω input source to the 200 Ω source impedance level for which the VGA was designed. This pad provides a very broadband input match at the expense of an 11.46 dB power attenuation in the input path. It is very important to take this into account when measuring the noise and distortion performance of the unmodified board using the IFIP input; the apparent noise figure will be degraded by 11.46 dB, and the apparent IIP3 will be 11.46 dB higher than actual. If full weak-signal performance is desired from the evaluation board, the attenuator (comprising R31 and R32) should be removed and replaced with a low-loss RF transformer providing the desired 4:1 impedance ratio. When a transformer is used, IFIN should be ac-coupled to ground and not driven differentially with IFIP.

MX Input

The evaluation board is by default set for a differential MX drive through a balun (T41) from a single-ended source fed into the MXIP SMA connector. When the MX inputs are used, the internal VGA is bypassed. To change to a differential driving source, T41 should be removed along with Resistor R42. The 0 Ω R43 and R44 resistors should be installed in place of T41 to bridge the gap between the input traces. This presents a nominal

differential impedance of 200 Ω (100 Ω per side). The differential inputs should then be fed into SMA connectors MXIP and MXIN.

Mixer Outputs

The I and Q mixer outputs are available through the IMXO and QMXO SMA connectors. These outputs are biased to VCMO and are not designed to drive loads smaller than 200 Ω. To prevent damage to test equipment that cannot tolerate dc biases, pads for series dc-blocking capacitors are provided. These pads are populated with 0 Ω by default.

Baseband Outputs

The baseband outputs are made available at the IOPP, IOPN, QOPP, and QOPN test points and SMA connectors. These outputs are not designed to be connected directly to 50 Ω loads and should be presented with loads of approximately 2 kΩ or greater.

The dc bias level of the baseband amplifier outputs are by default tied to VREF through LK11. If desired, the dc bias level can be changed by removing LK11 and driving a dc voltage onto the VCMO test point.

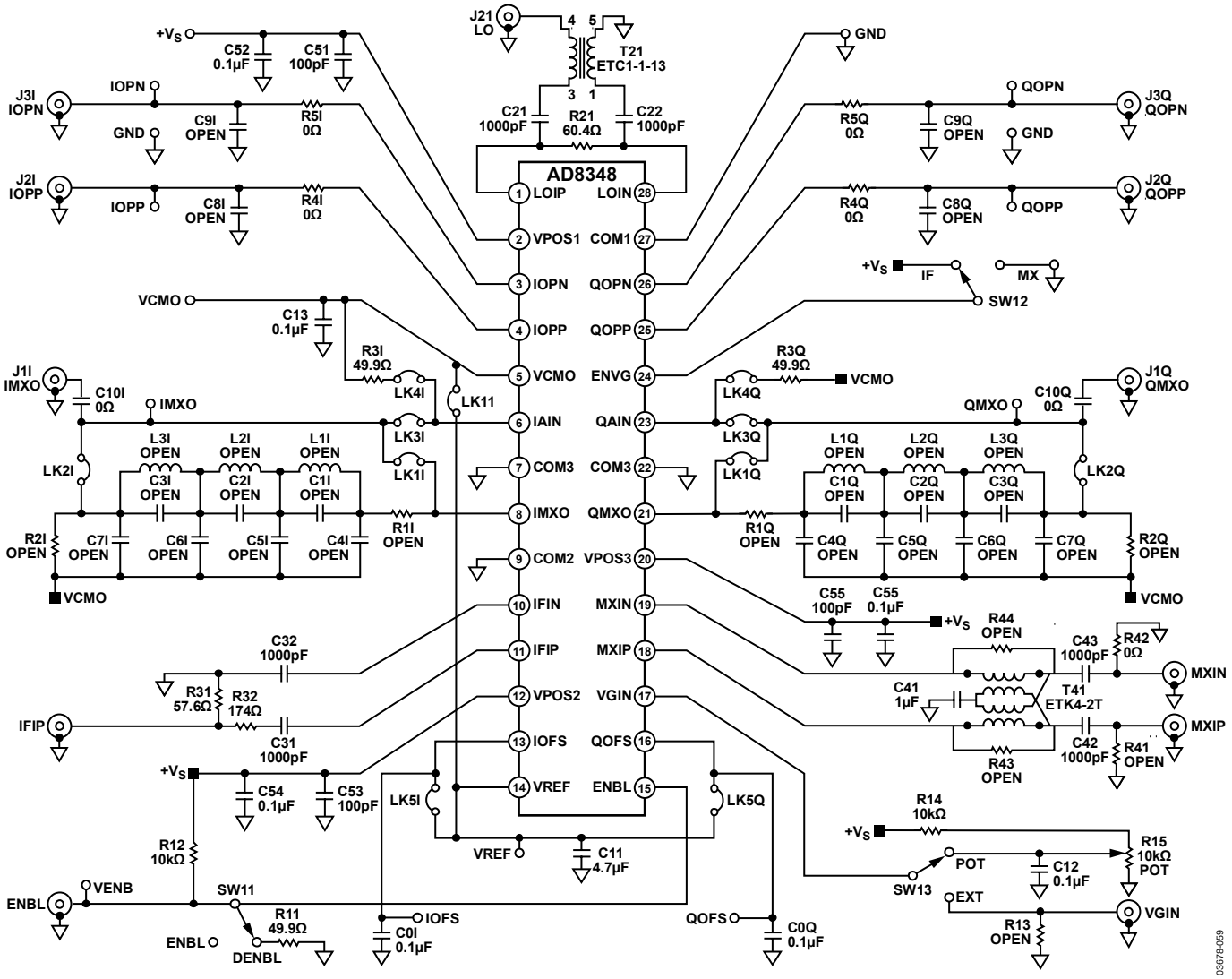
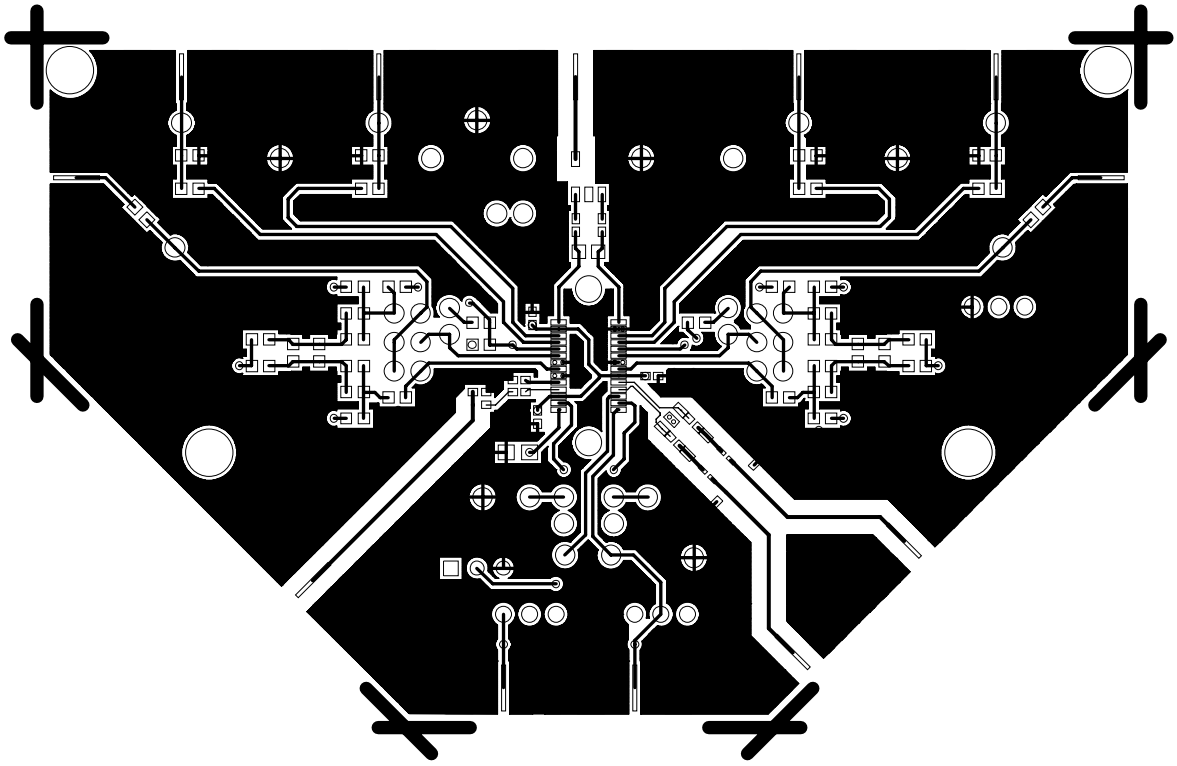
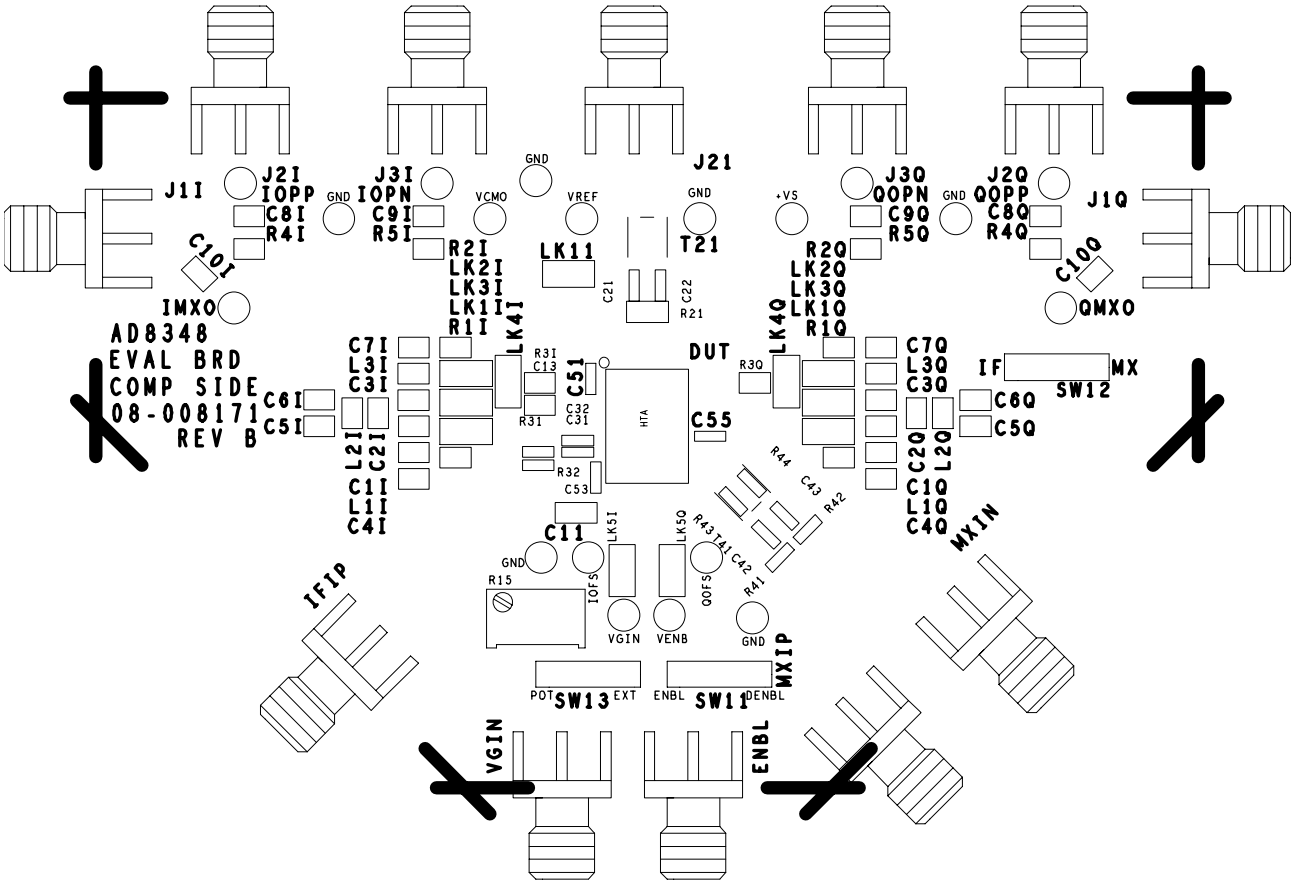


Figure 60. Evaluation Board Schematic



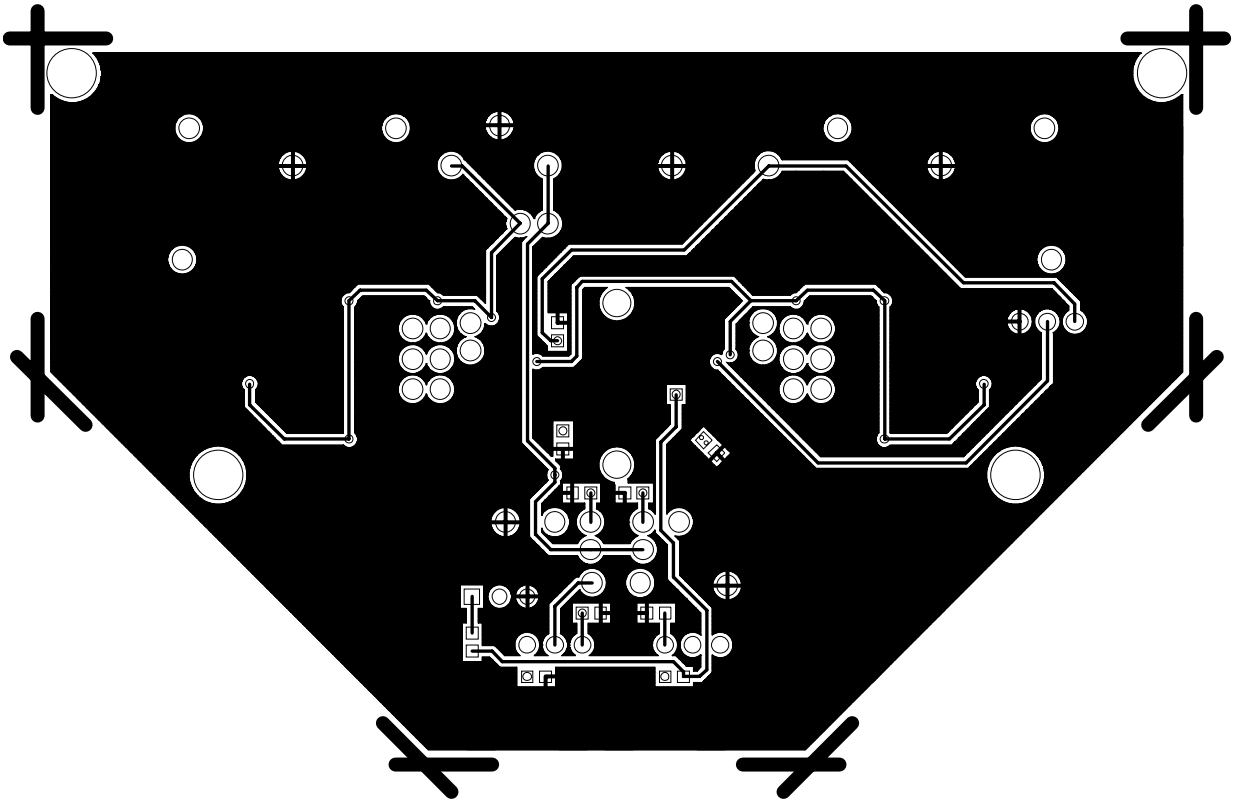
03678-060

Figure 61. Evaluation Board Top Layer



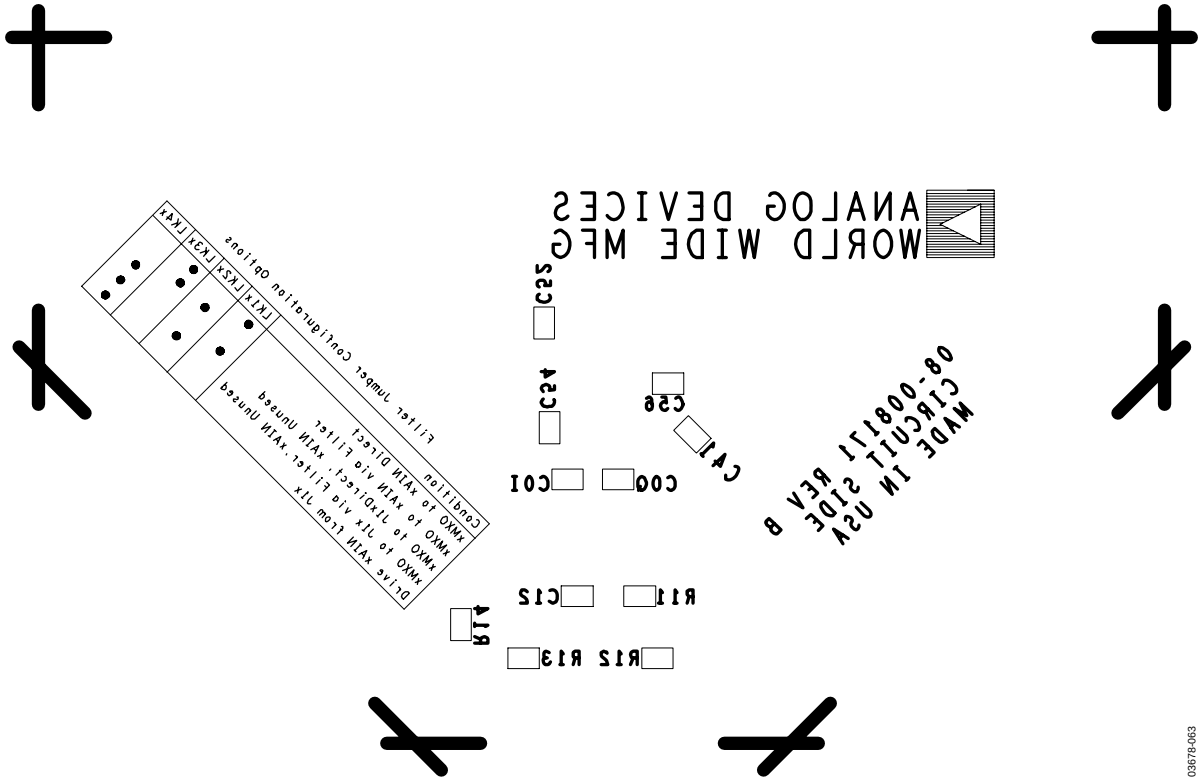
03678-061

Figure 62. Evaluation Board Top Silkscreen



03678-062

Figure 63. Evaluation Board Bottom Layer



03678-063

Figure 64. Evaluation Board Bottom Silkscreen

Table 6. Evaluation Board Configuration Options

Component	Function	Default Condition
V_S, GND	Power supply and ground vector pins.	Not applicable
SW11, ENBL	Device enable: Place SW11 in the ENBL position to connect the ENBL pin to V_S. Place SW11 in the DENBL position to disable the device by grounding the Pin ENBL through a 50 Ω pull-down resistor. The device can also be enabled via an external voltage applied to ENBL or VENB.	SW11 = ENBL
SW13, R15, VGIN	Gain control selection: With SW13 in the POT position, the gain of the VGA can be set using the R15 potentiometer. With SW13 in the EXT position, the VGA gain can be set by an external voltage to the SMA connector VGIN. For VGA operation, the VGA must first be enabled by setting SW12 to the IF position.	SW13 = POT
SW12	VGA enable selection: With SW12 in the IF position, the ENVG pin is connected to V_S and the VGA is enabled. The IF input should be used when SW12 is in the IF position. With SW12 in the MX position, the ENVG pin is grounded and the VGA is disabled. The MX inputs should be used when SW12 is in the MX position.	SW12 = IF
IFIP, R31, R32	IF inputs: The single-ended IF signal should be connected to this SMA connector. R31 and R32 form an L pad that presents a 50 Ω termination to the driving source. This L pad introduces an 11.46 dB loss in the input signal path and should be taken into consideration when calculating the gain of the AD8348.	R31 = 57.6 Ω R32 = 174 Ω
MXIP, MXIN, T41, R41, R42, C42, C43	Mixer inputs: These inputs can be configured for either differential or single-ended operation. The evaluation board is by default set for differential MX drive through a balun (T41) from a single-ended source fed into the MXIP SMA connector. To change to a differential driving source, T41 should be removed along with Resistor R42. The 0 Ω Resistors R43 and R44 should be installed in place of T41 to bridge the gap between the input traces. This will present a nominal differential impedance of 200 Ω (100 Ω per side). The differential inputs should then be fed into SMA connectors MXIP and MXIN.	T41 = M/A-COM ETK4-2T; R41= OPEN; C42, C43 = 1000 pF; R42 = 0 Ω
LK11, VCMO	Baseband amplifier output bias: Installing LK11 connects VREF to VCMO. This sets the bias level on the baseband amplifiers to VREF, which is equal to approximately 1 V. Alternatively, with LK11 removed, the bias level of the baseband amplifiers can be set by applying an external voltage to the VCMO test point.	LK11 installed
C8, C9, R4, R5 (I and Q)	Baseband amplifier outputs and output filter: Additional low-pass filtering can be provided at the baseband output with these filters.	R4, R5 = 0 Ω
C10 (I and Q)	Mixer output dc-blocking capacitors: The mixer outputs are biased to VCMO. To prevent damage to test equipment that cannot tolerate dc biases, C10 is provided to block the dc component, thus protecting the test equipment.	C10 = 0 Ω
C1 to C7, R1, R2, L1 to L3 (I and Q)	Baseband filter: These components are provided for baseband filtering between the mixer outputs and the baseband amplifier inputs. The baseband amplifier input impedance is high and the filter termination impedance is set by R2. See Table 7 for the jumper settings.	All = OPEN
LK5 (I and Q)	Offset compensation loop disable: Installing these jumpers will disable the offset compensation loop for the corresponding channel.	LK5x = OPEN

Table 7. Filter-Jumper Configuration Options

Condition	LK1x	LK2x	LK3x	LK4x
xMXO to xAIN Directly	•		•	
xMXO to xAIN via Filter		•	•	
xMXO to J1x Directly, xAIN Unused	•			•
xMXO to J1x via Filter, xAIN Unused		•		•
Drive xAIN from J1x				•

OUTLINE DIMENSIONS

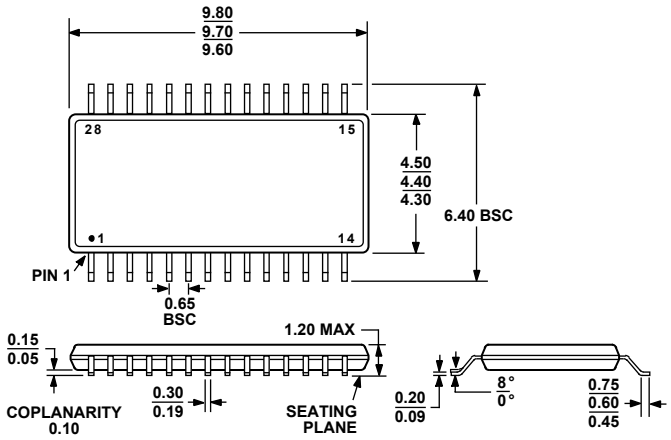


Figure 65. 28-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-28)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD8348ARU	−40°C to +85°C	28-Lead Thin Shrink Small Outline Package [TSSOP]	RU-28
AD8348ARU-REEL7	−40°C to +85°C	28-Lead Thin Shrink Small Outline Package [TSSOP] 7″Tape and Reel	RU-28
AD8348ARUZ[1]	−40°C to +85°C	28-Lead Thin Shrink Small Outline Package [TSSOP]	RU-28
AD8348ARUZ-REEL7[1]	−40°C to +85°C	28-Lead Thin Shrink Small Outline Package [TSSOP] 7″Tape and Reel	RU-28
AD8348-EVAL		Evaluation Board	

[1] Z = Pb-free part.

LF–2.7 GHz RF/IF Gain and Phase Detector

AD8302

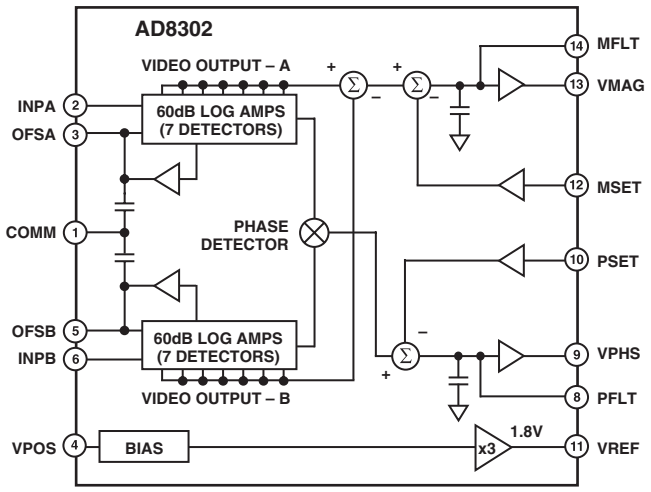
FEATURES

- Measures Gain/Loss and Phase up to 2.7 GHz
- Dual Demodulating Log Amps and Phase Detector
- Input Range –60 dBm to 0 dBm in a 50 Ω System
- Accurate Gain Measurement Scaling (30 mV/dB)
  - Typical Nonlinearity < 0.5 dB
- Accurate Phase Measurement Scaling (10 mV/Degree)
  - Typical Nonlinearity < 1 Degree
- Measurement/Controller/Level Comparator Modes
- Operates from Supply Voltages of 2.7 V–5.5 V
- Stable 1.8 V Reference Voltage Output
- Small Signal Envelope Bandwidth from DC to 30 MHz

APPLICATIONS

- RF/IF PA Linearization
- Precise RF Power Control
- Remote System Monitoring and Diagnostics
- Return Loss/VSWR Measurements
- Log Ratio Function for AC Signals

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD8302 is a fully integrated system for measuring gain/loss and phase in numerous receive, transmit, and instrumentation applications. It requires few external components and a single supply of 2.7 V–5.5 V. The ac-coupled input signals can range from –60 dBm to 0 dBm in a 50 Ω system, from low frequencies up to 2.7 GHz. The outputs provide an accurate measurement of either gain or loss over a ±30 dB range scaled to 30 mV/dB, and of phase over a 0°–180° range scaled to 10 mV/degree. Both subsystems have an output bandwidth of 30 MHz, which may optionally be reduced by the addition of external filter capacitors. The AD8302 can be used in controller mode to force the gain and phase of a signal chain toward predetermined setpoints.

The AD8302 comprises a closely matched pair of demodulating logarithmic amplifiers, each having a 60 dB measurement range. By taking the difference of their outputs, a measurement of the magnitude ratio or gain between the two input signals is available. These signals may even be at different frequencies, allowing the measurement of conversion gain or loss. The AD8302 may be used to determine absolute signal level by applying the unknown signal to one input and a calibrated ac reference signal to the other. With the output stage feedback connection disabled, a comparator may be realized, using the setpoint pins MSET and PSET to program the thresholds.

The signal inputs are single-ended, allowing them to be matched and connected directly to a directional coupler. Their input impedance is nominally 3 kΩ at low frequencies.

The AD8302 includes a phase detector of the multiplier type, but with precise phase balance driven by the fully limited signals appearing at the outputs of the two logarithmic amplifiers. Thus, the phase accuracy measurement is independent of signal level over a wide range.

The phase and gain output voltages are simultaneously available at loadable ground referenced outputs over the standard output range of 0 V to 1.8 V. The output drivers can source or sink up to 8 mA. A loadable, stable reference voltage of 1.8 V is available for precise repositioning of the output range by the user.

In controller applications, the connection between the gain output pin VMAG and the setpoint control pin MSET is broken. The desired setpoint is presented to MSET and the VMAG control signal drives an appropriate external variable gain device. Likewise, the feedback path between the phase output pin VPHS and its setpoint control pin PSET may be broken to allow operation as a phase controller.

The AD8302 is fabricated on Analog Devices' proprietary, high performance 25 GHz SOI complementary bipolar IC process. It is available in a 14-lead TSSOP package and operates over a –40°C to +85°C temperature range. An evaluation board is available.

REV. A

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329–4700 www.analog.com
Fax: 781/326-8703

AD8302–SPECIFICATIONS (T_A = 25°C, V_S = 5 V, VMAG shorted to MSET, VPHS shorted to PSET, 52.3 Ω shunt resistors connected to INPA and INPB, for Phase measurement $P_{INPA} = P_{INPB}$, unless otherwise noted.)

Parameter	Conditions	Min	Typ	Max	Unit
OVERALL FUNCTION					
Input Frequency Range		>0		2700	MHz
Gain Measurement Range	P_{IN} at INPA, P_{IN} at INPB = –30 dBm		±30		dB
Phase Measurement Range	ϕ_{IN} at INPA > ϕ_{IN} at INPB		±90		Degree
Reference Voltage Output	Pin VREF, –40°C ≤ T_A ≤ +85°C	1.72	1.8	1.88	V
INPUT INTERFACE	Pins INPA and INPB				
Input Simplified Equivalent Circuit	To AC Ground, f ≤ 500 MHz		3‖2		kΩ‖pF
Input Voltage Range	AC-Coupled (0 dBV = 1 V rms)	–73		–13	dBV
	re: 50 Ω	–60		0	dBm
Center of Input Dynamic Range			–43		dBV
			–30		dBm
MAGNITUDE OUTPUT	Pin VMAG				
Output Voltage Minimum	20 × Log (V_{INPA}/V_{INPB}) = –30 dB		30		mV
Output Voltage Maximum	20 × Log (V_{INPA}/V_{INPB}) = +30 dB		1.8		V
Center Point of Output (MCP)	$V_{INPA} = V_{INPB}$		900		mV
Output Current	Source/Sink		8		mA
Small Signal Envelope Bandwidth	Pin MFLT Open		30		MHz
Slew Rate	40 dB Change, Load 20 pF‖10 kΩ		25		V/µs
Response Time					
Rise Time	Any 20 dB Change, 10%–90%		50		ns
Fall Time	Any 20 dB Change, 90%–10%		60		ns
Settling Time	Full-Scale 60 dB Change, to 1% Settling		300		ns
PHASE OUTPUT	Pin VPHS				
Output Voltage Minimum	Phase Difference 180 Degrees		30		mV
Output Voltage Maximum	Phase Difference 0 Degrees		1.8		V
Phase Center Point	When $\phi_{INPA} = \phi_{INPB} \pm 90°$		900		mV
Output Current Drive	Source/Sink		8		mA
Slew Rate			25		V/µs
Small Signal Envelope Bandwidth			30		MHz
Response Time	Any 15 Degree Change, 10%–90%		40		ns
	120 Degree Change C_{FILT} = 1 pF, to 1% Settling		500		ns
100 MHz	MAGNITUDE OUTPUT				
Dynamic Range	±1 dB Linearity P_{REF} = –30 dBm (V_{REF} = –43 dBV)		58		dB
	±0.5 dB Linearity P_{REF} = –30 dBm (V_{REF} = –43 dBV)		55		dB
	±0.2 dB Linearity P_{REF} = –30 dBm (V_{REF} = –43 dBV)		42		dB
Slope	From Linear Regression		29		mV/dB
Deviation vs. Temperature	Deviation from Output at 25°C				
	–40°C ≤ T_A ≤ +85°C, $P_{INPA} = P_{INPB}$ = –30 dBm		0.25		dB
	Deviation from Best Fit Curve at 25°C				
	–40°C ≤ T_A ≤ +85°C, P_{INPA} = ±25 dB, P_{INPB} = –30 dBm		0.25		dB
Gain Measurement Balance	$P_{INPA} = P_{INPB}$ = –5 dBm to –50 dBm		0.2		dB
	PHASE OUTPUT				
Dynamic Range	Less than ±1 Degree Deviation from Best Fit Line		145		Degree
	Less than 10% Deviation in Instantaneous Slope		143		Degree
Slope (Absolute Value)	From Linear Regression about –90° or +90°		10		mV/Degree
Deviation vs. Temperature	Deviation from Output at 25°C				
	–40°C ≤ T_A ≤ +85°C, Delta Phase = 90 Degrees		0.7		Degree
	Deviation from Best Fit Curve at 25°C				
	–40°C ≤ T_A ≤ +85°C, Delta Phase = ±30 Degrees		0.7		Degree

Parameter	Conditions	Min	Typ	Max	Unit
900 MHz	MAGNITUDE OUTPUT				
Dynamic Range	±1 dB Linearity P_{REF} = –30 dBm (V_{REF} = –43 dBV)		58		dB
	±0.5 dB Linearity P_{REF} = –30 dBm (V_{REF} = –43 dBV)		54		dB
	±0.2 dB Linearity P_{REF} = –30 dBm (V_{REF} = –43 dBV)		42		dB
Slope	From Linear Regression		28.7		mV/dB
Deviation vs. Temperature	Deviation from Output at 25°C				
	–40°C ≤ T_A ≤ +85°C, P_{INPA} = P_{INPB} = –30 dBm		0.25		dB
	Deviation from Best Fit Curve at 25°C				
	–40°C ≤ T_A ≤ +85°C, P_{INPA} = ±25 dB, P_{INPB} = –30 dBm		0.25		dB
Gain Measurement Balance	P_{INPA} = P_{INPB} = –5 dBm to –50 dBm		0.2		dB
	PHASE OUTPUT				
Dynamic Range	Less than ± 1 Degree Deviation from Best Fit Line		143		Degree
	Less than 10% Deviation in Instantaneous Slope		143		Degree
Slope (Absolute Value)	From Linear Regression about –90° or +90°		10.1		mV/Degree
Deviation	Linear Deviation from Best Fit Curve at 25°C				
	–40°C ≤ T_A ≤ +85°C, Delta Phase = 90 Degrees		0.75		Degree
	–40°C ≤ T_A ≤ +85°C, Delta Phase = ±30 Degrees		0.75		Degree
Phase Measurement Balance	Phase @ INPA = Phase @ INPB, P_{IN} = –5 dBm to –50 dBm		0.8		Degree
1900 MHz	MAGNITUDE OUTPUT				
Dynamic Range	±1 dB Linearity P_{REF} = –30 dBm (V_{REF} = –43 dBV)		57		dB
	±0.5 dB Linearity P_{REF} = –30 dBm (V_{REF} = –43 dBV)		54		dB
	±0.2 dB Linearity P_{REF} = –30 dBm (V_{REF} = –43 dBV)		42		dB
Slope	From Linear Regression		27.5		mV/dB
Deviation vs. Temperature	Deviation from Output at 25°C				
	–40°C ≤ T_A ≤ +85°C, P_{INPA} = P_{INPB} = –30 dBm		0.27		dB
	Deviation from Best Fit Curve at 25°C				
	–40°C ≤ T_A ≤ +85°C, P_{INPA} = ±25 dB, P_{INPB} = –30 dBm		0.33		dB
Gain Measurement Balance	P_{INPA} = P_{INPB} = –5 dBm to –50 dBm		0.2		dB
	PHASE OUTPUT				
Dynamic Range	Less than ±1 Degree Deviation from Best Fit Line		128		Degree
	Less than 10% Deviation in Instantaneous Slope		120		Degree
Slope (Absolute Value)	From Linear Regression about –90° or +90°		10.2		mV/Degree
Deviation	Linear Deviation from Best Fit Curve at 25°C				
	–40°C ≤ T_A ≤ +85°C, Delta Phase = 90 Degrees		0.8		Degree
	–40°C ≤ T_A ≤ +85°C, Delta Phase = ±30 Degrees		0.8		Degree
Phase Measurement Balance	Phase @ INPA = Phase @ INPB, P_{IN} = –5 dBm to –50 dBm		1		Degree
2200 MHz	MAGNITUDE OUTPUT				
Dynamic Range	±1 dB Linearity P_{REF} = –30 dBm (V_{REF} = –43 dBV)		53		dB
	±0.5 dB Linearity P_{REF} = –30 dBm (V_{REF} = –43 dBV)		51		dB
	±0.2 dB Linearity P_{REF} = –30 dBm (V_{REF} = –43 dBV)		38		dB
Slope	From Linear Regression		27.5		mV/dB
Deviation vs. Temperature	Deviation from Output at 25°C				
	–40°C ≤ T_A ≤ +85°C, P_{INPA} = P_{INPB} = –30 dBm		0.28		dB
	Deviation from Best Fit Curve at 25°C				
	–40°C ≤ T_A ≤ +85°C, P_{INPA} = ±25 dB, P_{INPB} = –30 dBm		0.4		dB
Gain Measurement Balance	P_{INPA} = P_{INPB} = –5 dBm to –50 dBm		0.2		dB
	PHASE OUTPUT				
Dynamic Range	Less than ±1 Degree Deviation from Best Fit Line		115		Degree
	Less than 10% Deviation in Instantaneous Slope		110		Degree
Slope (Absolute Value)	From Linear Regression about –90° or +90°		10		mV/Degree
Deviation	Linear Deviation from Best Fit Curve at 25°C				
	–40°C ≤ T_A ≤ +85°C, Delta Phase = 90 Degrees		0.85		Degree
	–40°C ≤ T_A ≤ +85°C, Delta Phase = ±30 Degrees		0.9		Degree
REFERENCE VOLTAGE	Pin VREF				
Output Voltage	Load = 2 kΩ	1.7	1.8	1.9	V
PSRR	V_S = 2.7 V to 5.5 V		0.25		mV/V
Output Current	Source/Sink (Less than 1% Change)		5		mA
POWER SUPPLY	Pin VPOS				
Supply		2.7	5.0	5.5	V
Operating Current (Quiescent)	V_S = 5 V		19	25	mA
	–40°C ≤ T_A ≤ +85°C		21	27	mA

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

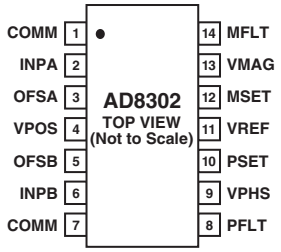
Supply Voltage V_S . . . . . 5.5 V
PSET, MSET Voltage . . . . . V_S + 0.3 V
INPA, INPB Maximum Input . . . . . –3 dBV
Equivalent Power Re. 50 Ω . . . . . 10 dBm
θ_{JA}[2] . . . . . 150°C/W
Maximum Junction Temperature . . . . . 125°C
Operating Temperature Range . . . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature Range (Soldering 60 sec) . . . . . 300°C

NOTES

[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]JEDEC 1S Standard (2-layer) board data.

PIN CONFIGURATION



PIN FUNCTION DESCRIPTIONS

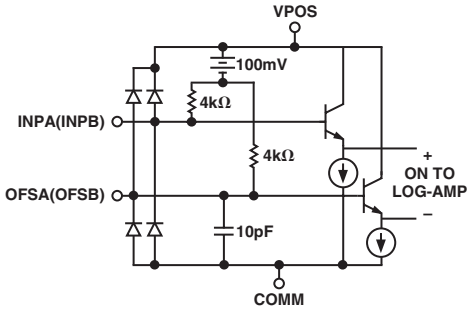
Pin No.	Mnemonic	Function	Equivalent Circuit
1, 7	COMM	Device Common. Connect to low impedance ground.	
2	INPA	High Input Impedance to Channel A. Must be ac-coupled.	Circuit A
3	OFSA	A capacitor to ground at this pin sets the offset compensation filter corner and provides input decoupling.	Circuit A
4	VPOS	Voltage Supply (V_S), 2.7 V to 5.5 V	
5	OFSB	A capacitor to ground at this pin sets the offset compensation filter corner and provides input decoupling.	Circuit A
6	INPB	Input to Channel B. Same structure as INPA.	Circuit A
8	PFLT	Low Pass Filter Terminal for the Phase Output	Circuit E
9	VPHS	Single-Ended Output Proportional to the Phase Difference between INPA and INPB.	Circuit B
10	PSET	Feedback Pin for Scaling of VPHS Output Voltage in Measurement Mode. Apply a setpoint voltage for controller mode.	Circuit D
11	VREF	Internally Generated Reference Voltage (1.8 V Nominal)	Circuit C
12	MSET	Feedback Pin for Scaling of VMAG Output Voltage Measurement Mode. Accepts a set point voltage in controller mode.	Circuit D
13	VMAG	Single-Ended Output. Output voltage proportional to the decibel ratio of signals applied to INPA and INPB.	Circuit B
14	MFLT	Low Pass Filter Terminal for the Magnitude Output	Circuit E

ORDERING GUIDE

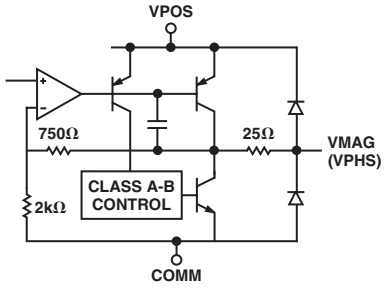
Model	Temperature Range	Package Description	Package Option
AD8302ARU	–40°C to +85°C	Tube, 14-Lead TSSOP	RU-14
AD8302ARU-REEL		13" Tape and Reel	
AD8302ARU-REEL7		7" Tape and Reel	
AD8302-EVAL		Evaluation Board	

CAUTION

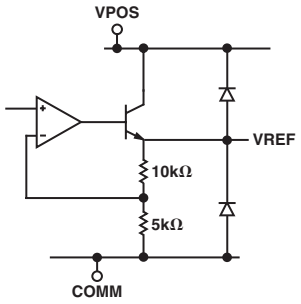
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8302 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



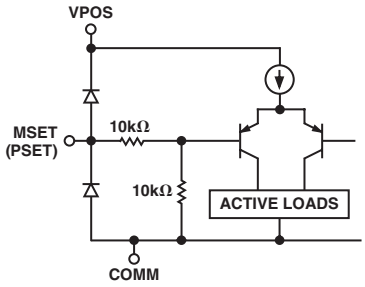
Circuit A



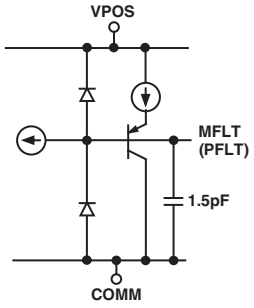
Circuit B



Circuit C



Circuit D

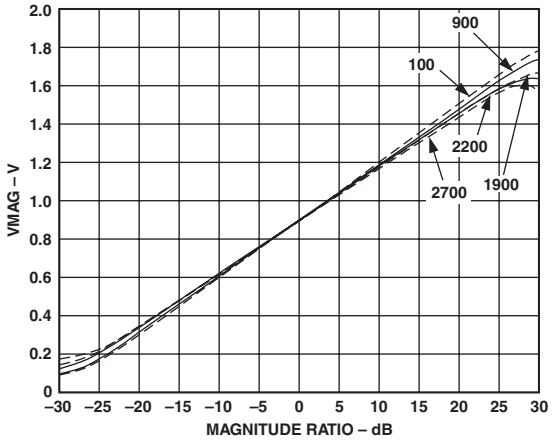


Circuit E

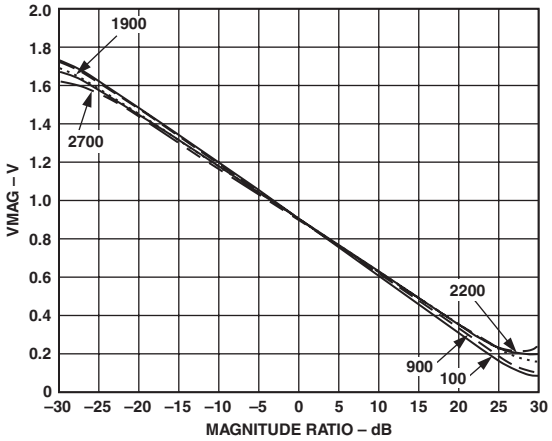
Figure 1. Equivalent Circuits

AD8302–Typical Performance Characteristics

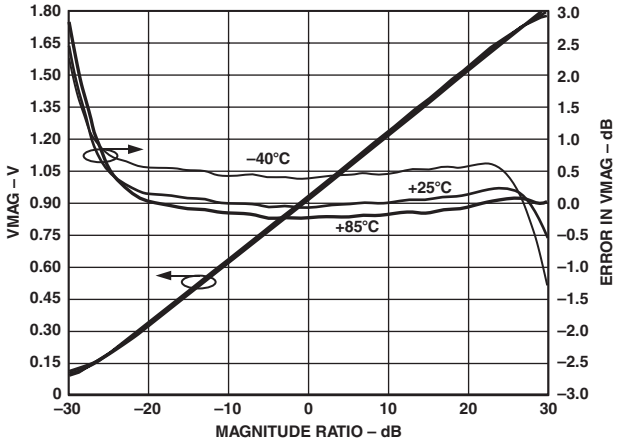
(V_S = 5 V, V_{INPB} is the reference input and V_{INPA} is swept, unless otherwise noted. All references to dBm are referred to 50 Ω. For the phase output curves, the input signal levels are equal, unless otherwise noted.)



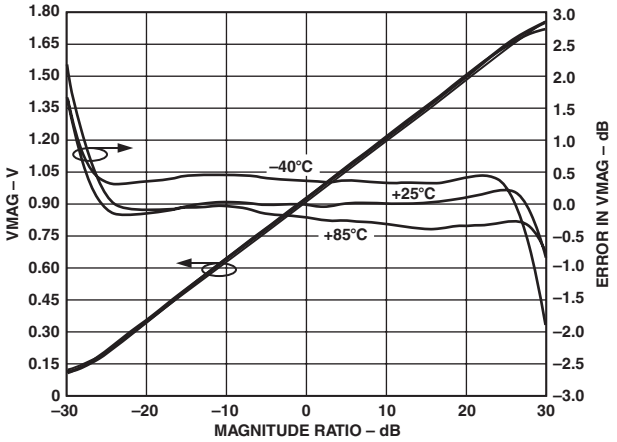
TPC 1. Magnitude Output (VMAG) vs. Input Level Ratio (Gain) V_{INPA}/V_{INPB}, Frequencies 100 MHz, 900 MHz, 1900 MHz, 2200 MHz, 2700 MHz, 25°C, P_{INPB} = –30 dBm, (Re: 50 Ω)



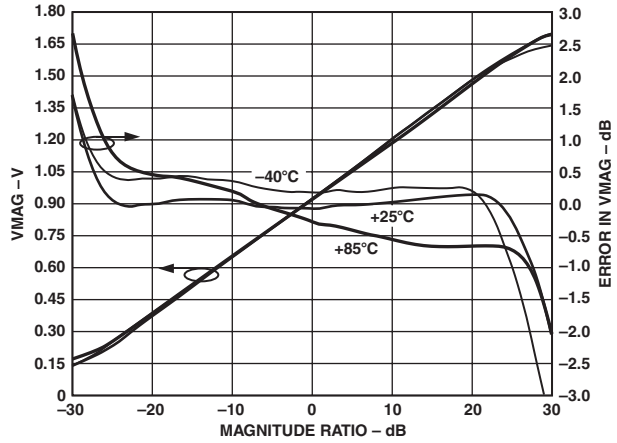
TPC 2. VMAG vs. Input Level Ratio (Gain) V_{INPA}/V_{INPB}, Frequencies 100 MHz, 900 MHz, 1900 MHz, 2200 MHz, 2700 MHz, P_{INPA} = –30 dBm



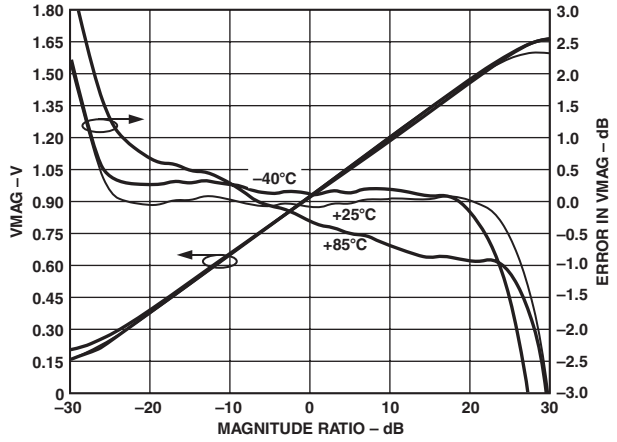
TPC 3. VMAG Output and Log Conformance vs. Input Level Ratio (Gain), Frequency 100 MHz, –40°C, +25°C, and +85°C, Reference Level = –30 dBm



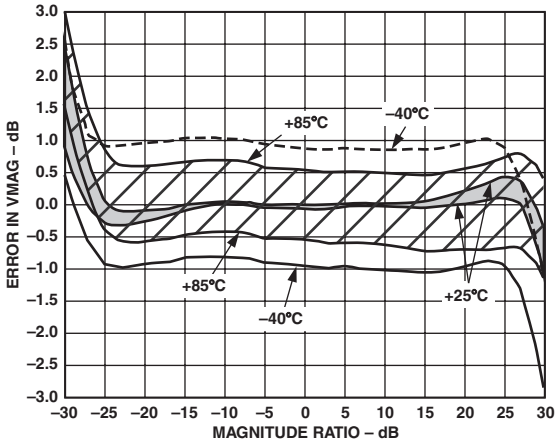
TPC 4. VMAG and Log Conformance vs. Input Level Ratio (Gain), Frequency 900 MHz, –40°C, +25°C, and +85°C, Reference Level = –30 dBm



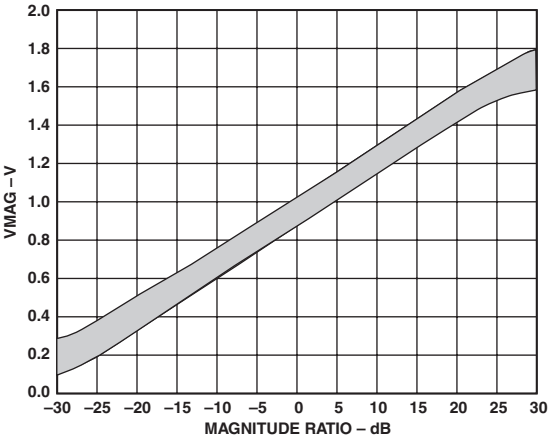
TPC 5. VMAG and Log Conformance vs. Input Level Ratio (Gain), Frequency 1900 MHz, –40°C, +25°C, and +85°C, Reference Level = –30 dBm



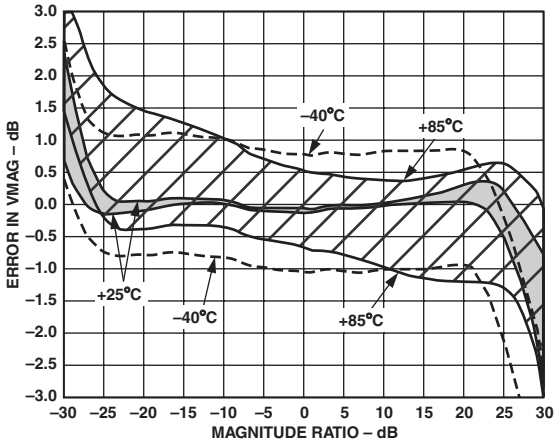
TPC 6. VMAG Output and Log Conformance vs. Input Level Ratio (Gain), Frequency 2200 MHz, –40°C, +25°C, and +85°C, Reference Level = –30 dBm



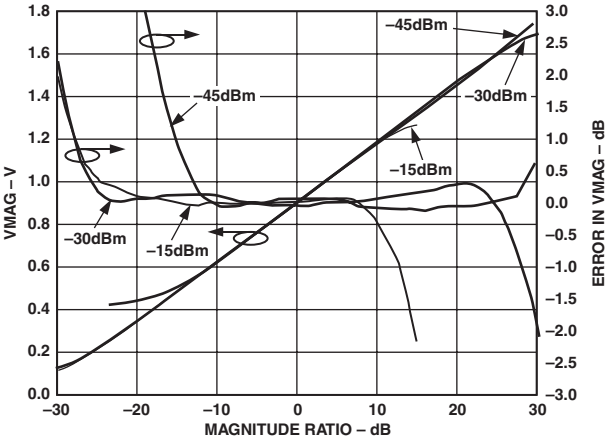
TPC 7. Distribution of Magnitude Error vs. Input Level Ratio (Gain), Three Sigma to Either Side of Mean, Frequency 900 MHz, –40°C, +25°C, and +85°C, Reference Level = –30 dBm



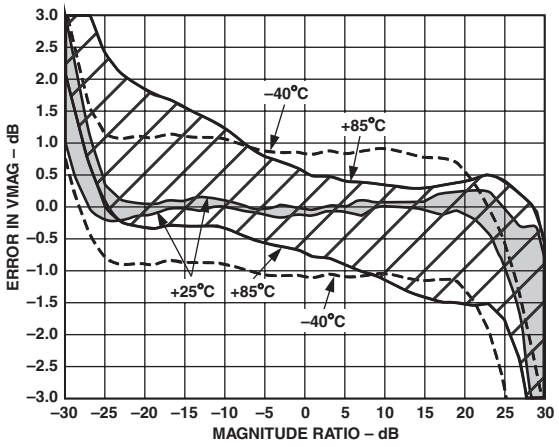
TPC 10. Distribution of VMAG vs. Input Level Ratio (Gain), Three Sigma to Either Side of Mean, Frequency 1900 MHz, Temperatures Between –40°C and +85°C, Reference Level = –30 dBm



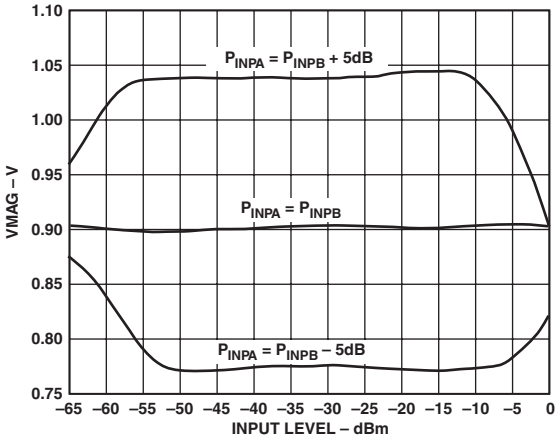
TPC 8. Distribution of Error vs. Input Level Ratio (Gain), Three Sigma to Either Side of Mean, Frequency 1900 MHz, –40°C, +25°C, and +85°C, Reference Level = –30 dBm



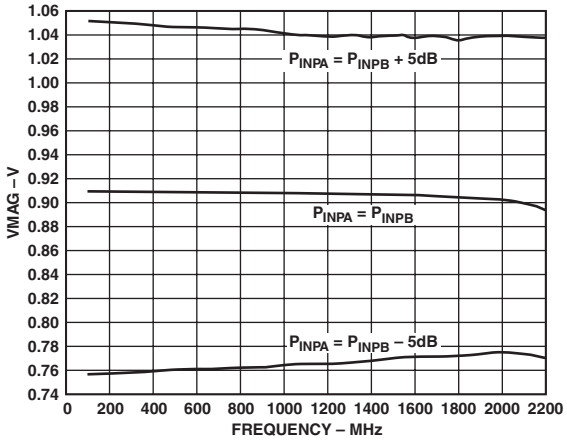
TPC 11. VMAG Output and Log Conformance vs. Input Level Ratio (Gain), Reference Level = –15 dBm, –30 dBm, and –45 dBm, Frequency 1900 MHz



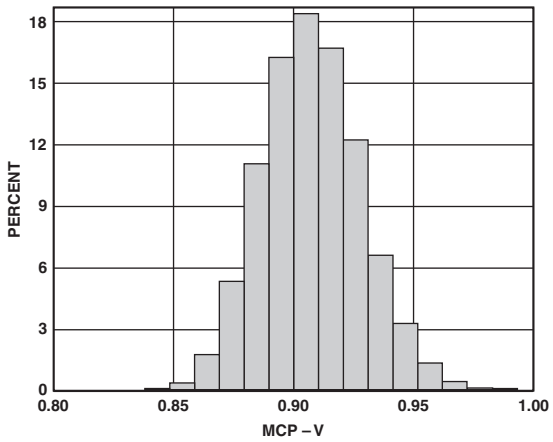
TPC 9. Distribution of Magnitude Error vs. Input Level Ratio (Gain), Three Sigma to Either Side of Mean, Frequency 2200 MHz, Temperatures –40°C, +25°C, and +85°C, Reference Level = –30 dBm



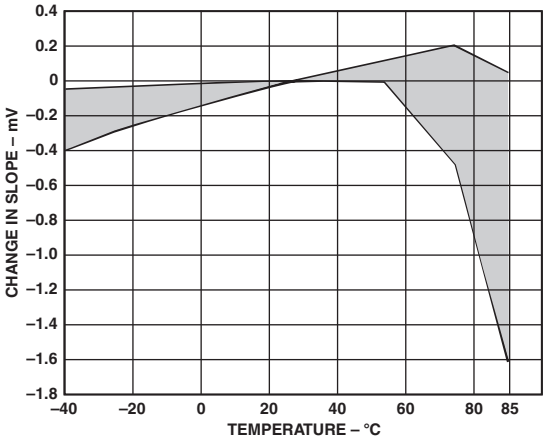
TPC 12. VMAG Output vs. Input Level for $P_{INPA} = P_{INPB}$, $P_{INPA} = P_{INPB} + 5$ dB, $P_{INPA} = P_{INPB} – 5$ dB, Frequency 1900 MHz



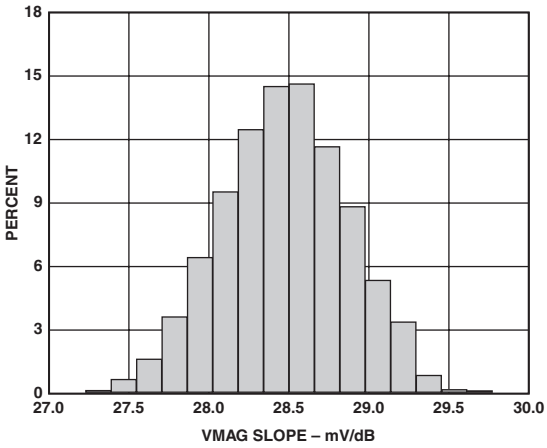
TPC 13. VMAG Output vs. Frequency, for $P_{INPA} = P_{INPB}$, $P_{INPA} = P_{INPB} + 5$ dB, and $P_{INPA} = P_{INPB} – 5$ dB, $P_{INPB} = –30$ dBm



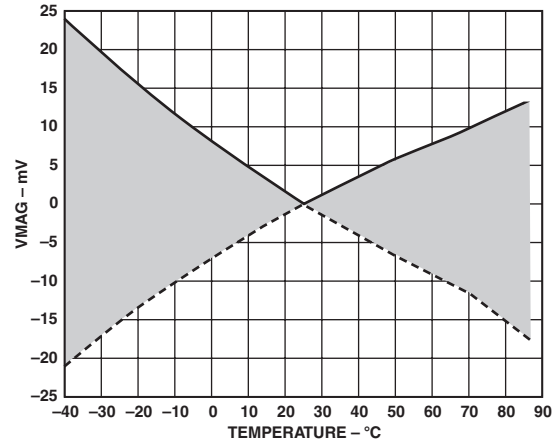
TPC 16. Center Point of Magnitude Output (MCP) Distribution Frequencies 900 MHz, 17,000 Units



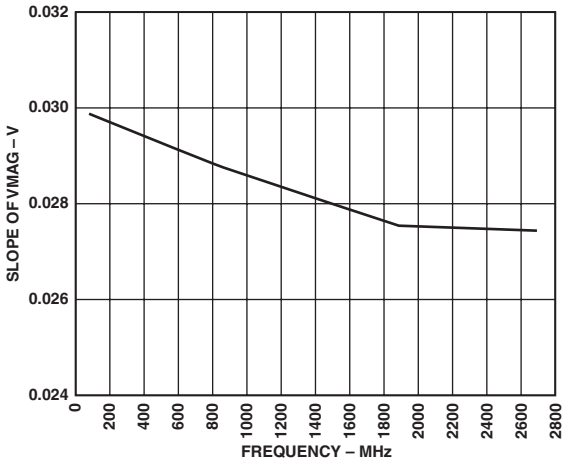
TPC 14. Change in VMAG Slope vs. Temperature, Three Sigma to Either Side of Mean, Frequencies 1900 MHz



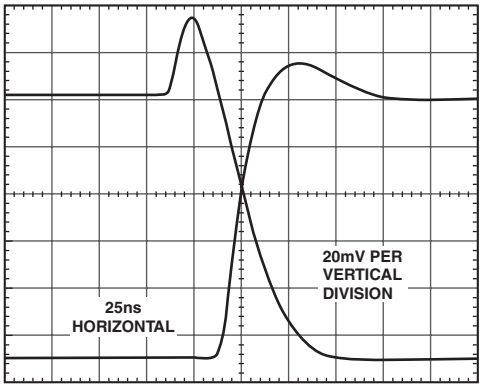
TPC 17. VMAG Slope, Frequency 900 MHz, 17,000 Units



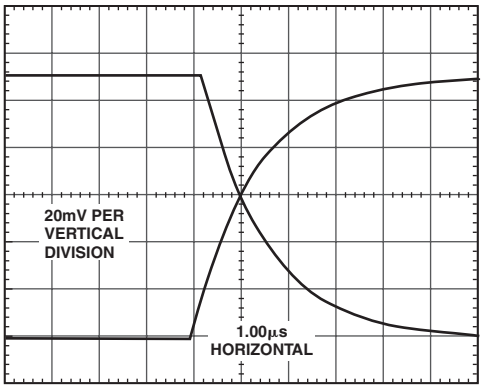
TPC 15. Change in Center Point of Magnitude Output (MCP) vs. Temperature, Three Sigma to Either Side of Mean, Frequencies 1900 MHz



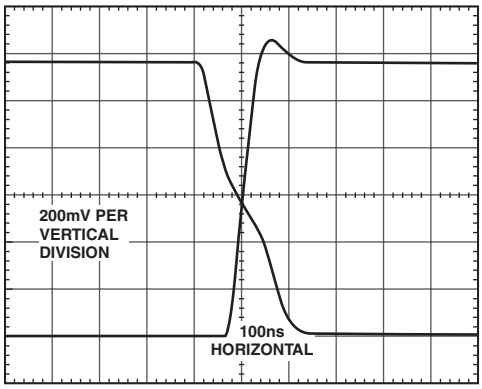
TPC 18. VMAG Slope vs. Frequency



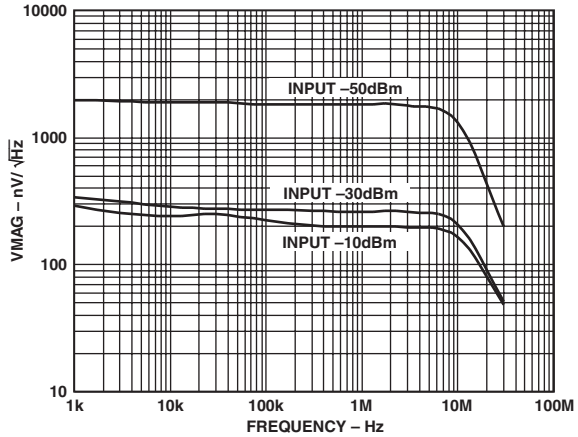
TPC 19. Magnitude Output Response to 4 dB Step, for P_{INPB} = –30 dBm, P_{INPA} = –32 dBm to –28 dBm, Frequency 1900 MHz, No Filter Capacitor



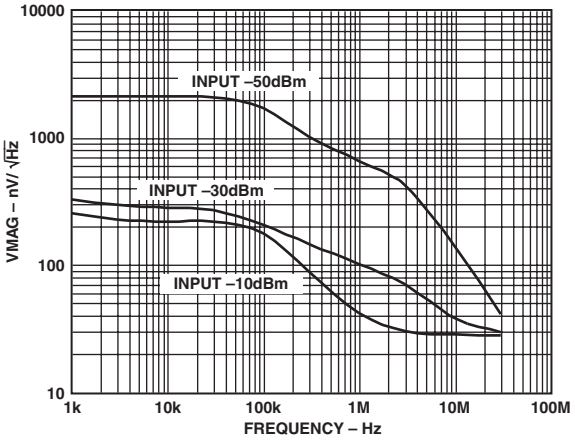
TPC 20. Magnitude Output Response to 4 dB Step, for P_{INPB} = –30 dBm, P_{INPA} = –32 dBm to –28 dBm, Frequency 1900 MHz, 1 nF Filter Capacitor



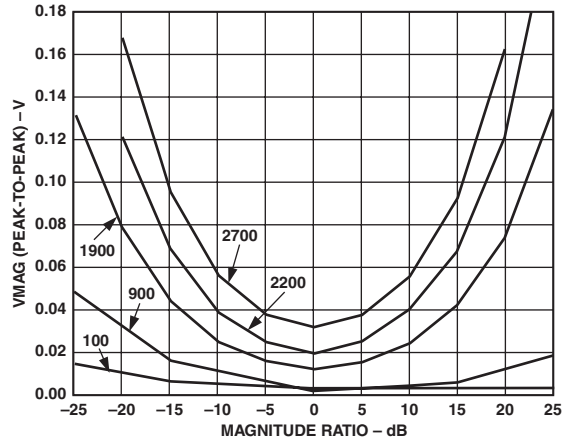
TPC 21. Magnitude Output Response to 40 dB Step, for P_{INPB} = –30 dBm, P_{INPA} = –50 dBm to –10 dBm, Supply 5 V, Frequency 1900 MHz, No Filter Capacitor



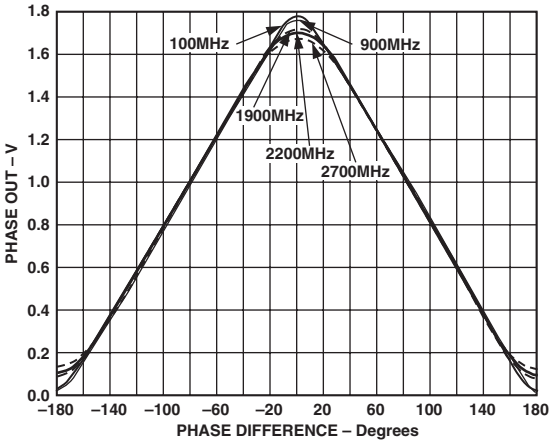
TPC 22. Magnitude Output Noise Spectral Density, P_{INPA} = P_{INPB} = –10 dBm, –30 dBm, –50 dBm, No Filter Capacitor



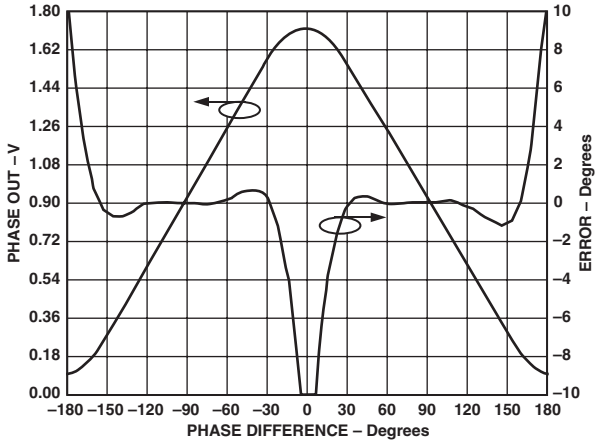
TPC 23. Magnitude Output Noise Spectral Density, P_{INPA} = P_{INPB} = –10 dBm, –30 dBm, –50 dBm, with Filter Capacitor, C = 1 nF



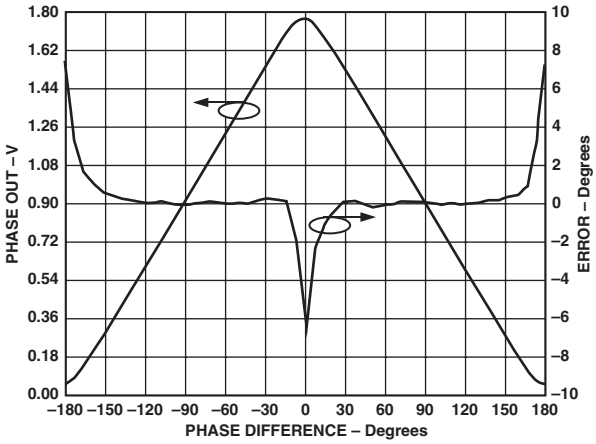
TPC 24. VMAG Peak-to-Peak Output Induced by Sweeping Phase Difference through 360 Degrees vs. Magnitude Ratio, Frequencies 100 MHz, 900 MHz, 1900 MHz, 2200 MHz, and 2700 MHz



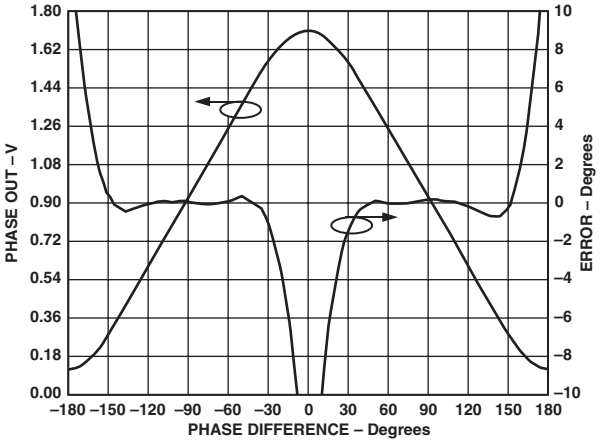
TPC 25. Phase Output (VPHS) vs. Input Phase Difference, Input Levels –30 dBm, Frequencies 100 MHz, 900 MHz, 1900 MHz, 2200 MHz, Supply 5 V, 2700 MHz



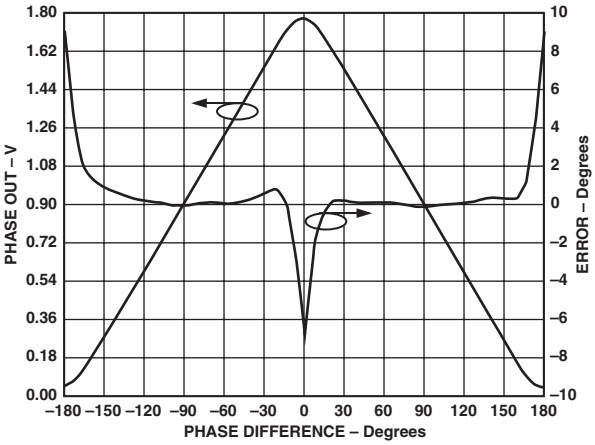
TPC 28. VPHS Output and Nonlinearity vs. Input Phase Difference, Input Levels –30 dBm, Frequency 1900 MHz



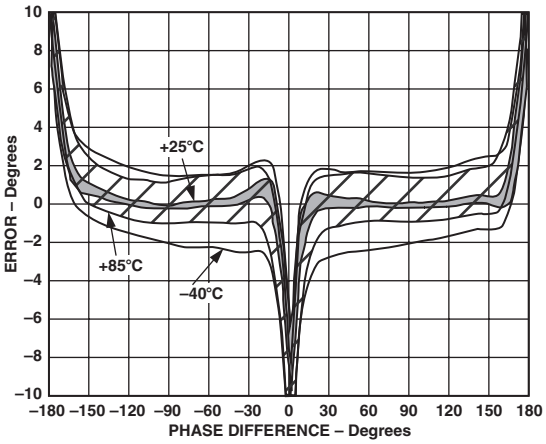
TPC 26. VPHS Output and Nonlinearity vs. Input Phase Difference, Input Levels –30 dBm, Frequency 100 MHz



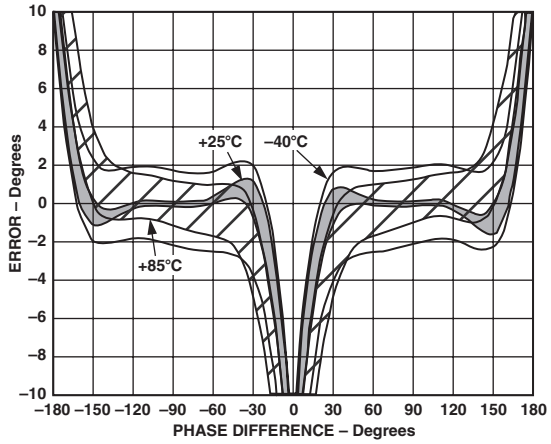
TPC 29. VPHS Output and Nonlinearity vs. Input Phase Difference, Input Levels –30 dBm, Frequency 2200 MHz



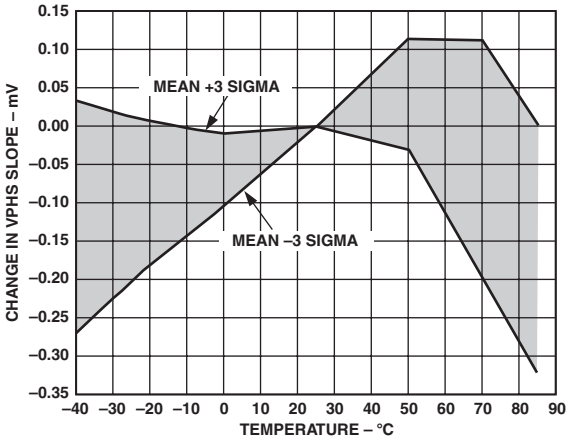
TPC 27. VPHS Output and Nonlinearity vs. Input Phase Difference, Input Levels –30 dBm, Frequency 900 MHz



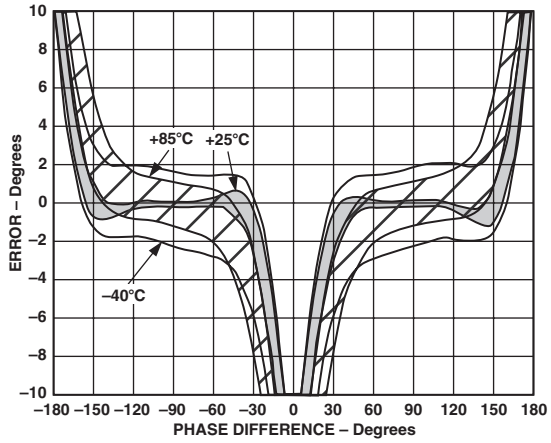
TPC 30. Distribution of VPHS Error vs. Input Phase Difference, Three Sigma to Either Side of Mean, Frequency 900 MHz, –40°C, +25°C, and +85°C, Input Levels –30 dBm



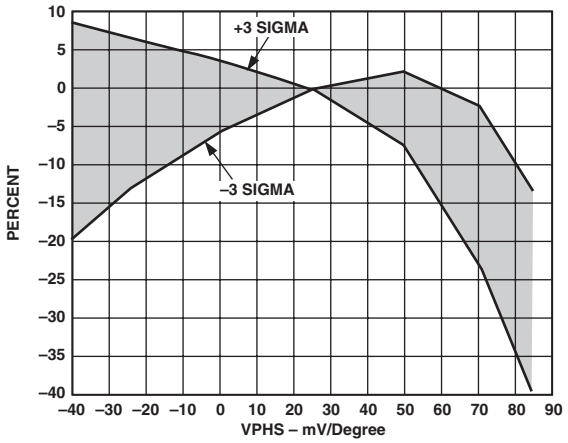
TPC 31. Distribution of VPHS Error vs. Input Phase Difference, Three Sigma to Either Side of Mean, Frequency 1900 MHz, –40°C, +25°C, and +85°C, Supply 5 V, Input Levels P_{INPA} = P_{INPB} = –30 dBm



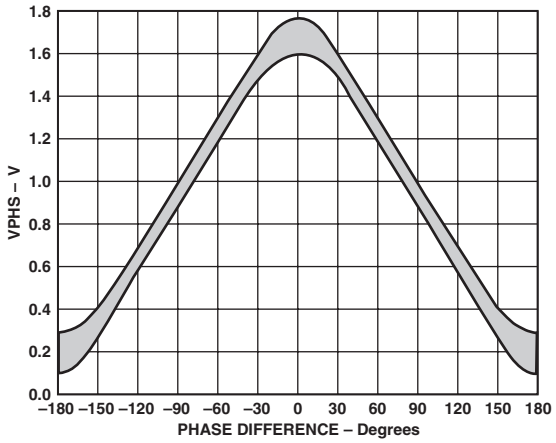
TPC 34. Change in VPHS Slope vs. Temperature, Three Sigma to Either Side of Mean, Frequency 1900 MHz



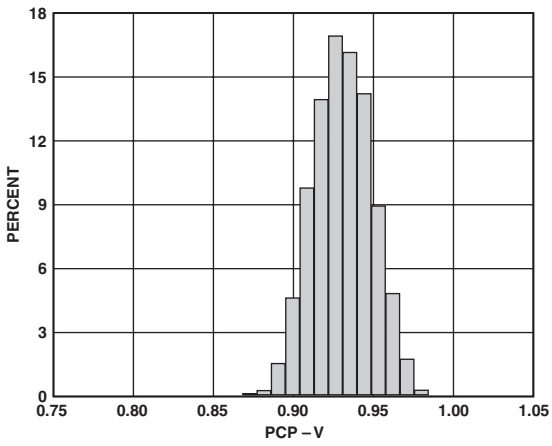
TPC 32. Distribution of VPHS Error vs. Input Phase Difference, Three Sigma to Either Side of Mean, Frequency 2200 MHz, –40°C, +25°C, and +85°C, Input Levels –30 dBm



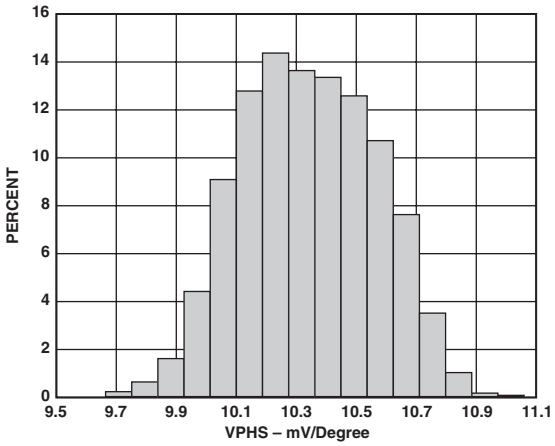
TPC 35. Change in Phase Center Point (PCP) vs. Temperature, Three Sigma to Either Side of Mean, Frequency 1900 MHz



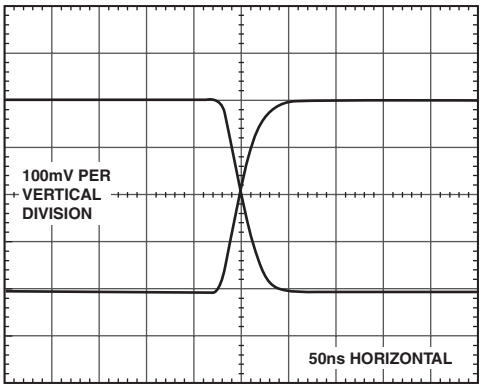
TPC 33. Distribution of VPHS vs. Input Phase Difference, Three Sigma to Either Side of Mean, Frequency 900 MHz, Temperature between –40°C and +85°C, Input Levels –30 dBm



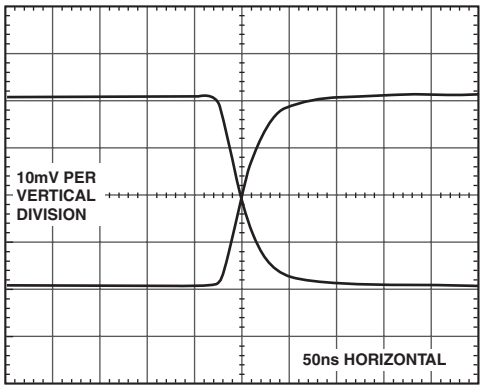
TPC 36. Phase Center Point (PCP) Distribution, Frequency 900 MHz, 17,000 Units



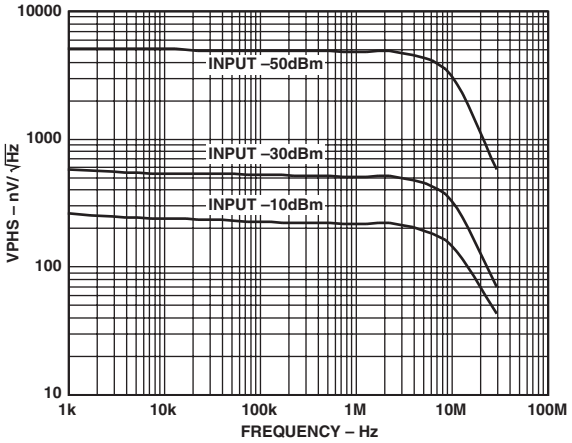
TPC 37. VPHS Slope Distribution, Frequency 900 MHz



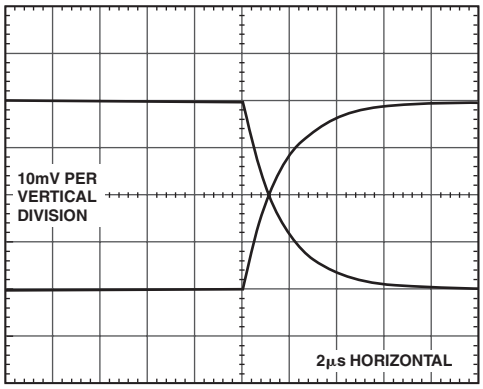
TPC 40. VPHS Output Response to 40° Step with Nominal Phase Shift of 90°, Input Levels P_{INPA} = P_{INPB} = –30 dBm, Frequency 1900 MHz,1 pF Filter Capacitor



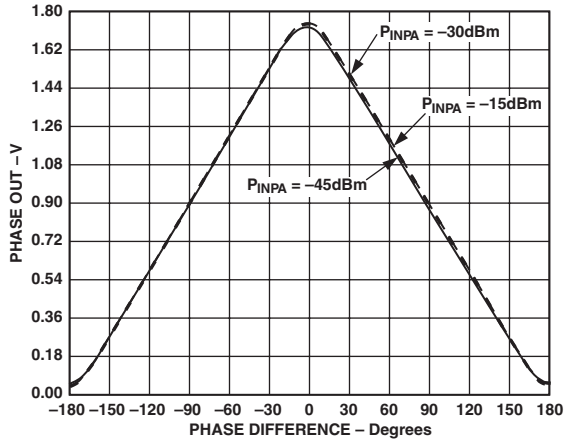
TPC 38. VPHS Output Response to 4° Step with Nominal Phase Shift of 90°, Input Levels –30 dBm, Frequency 1900 MHz, 25°C, 1 pF Filter Capacitor



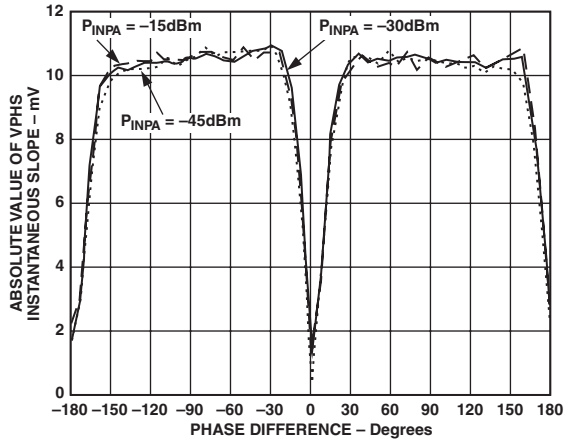
TPC 41. VPHS Output Noise Spectral Density vs. Frequency, P_{INPA} = –30 dBm, P_{INPB} = –10 dBm, –30 dBm, –50 dBm, and 90° Input Phase Difference



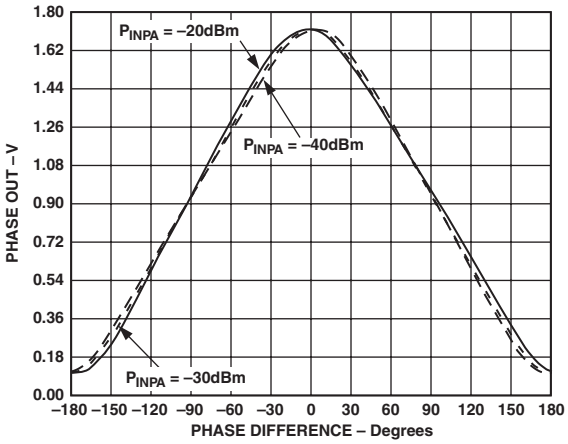
TPC 39. VPHS Output Response to 4° Step with Nominal Phase Shift of 90°, Input Levels P_{INPA} = P_{INPB} = –30 dBm, Supply 5 V, Frequency 1900 MHz, 25°C, with 100 pF Filter Capacitor



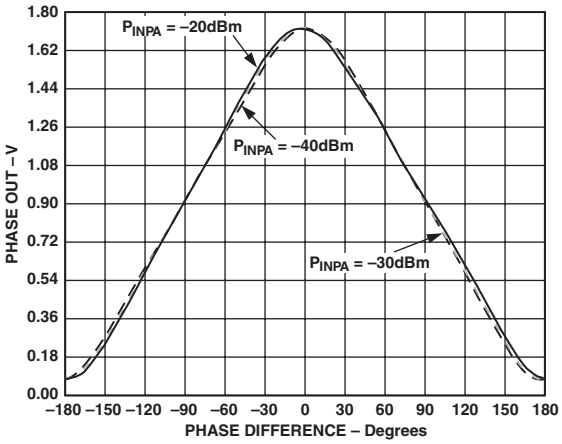
TPC 42. Phase Output vs. Input Phase Difference, P_{INPA} = P_{INPB}, P_{INPA} = P_{INPB} + 15 dB, P_{INPA} = P_{INPB} – 15 dB, Frequency 900 MHz



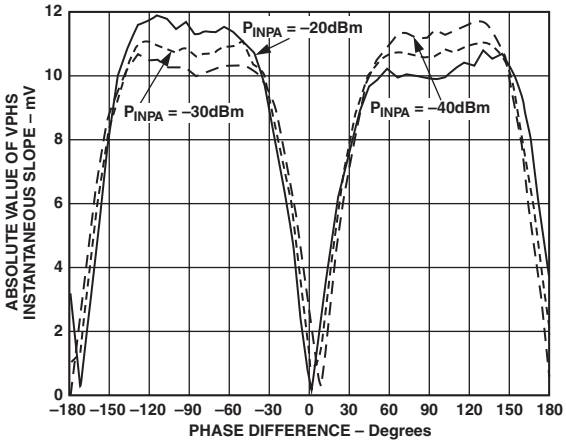
TPC 43. Phase Output Instantaneous Slope, $P_{INPA} = P_{INPB}$, $P_{INPA} = P_{INPB}$ + 15 dB, $P_{INPA} = P_{INPB}$ – 15 dB, Frequency 900 MHz



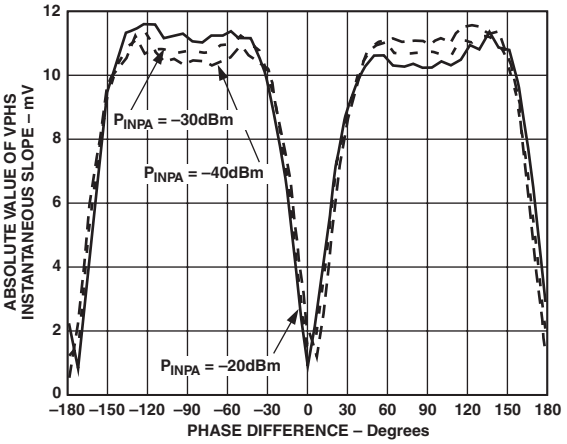
TPC 46. Phase Output vs. Input Phase Difference, $P_{INPA} = P_{INPB}$, $P_{INPA} = P_{INPB}$ + 10 dB, $P_{INPA} = P_{INPB}$ – 10 dB, Frequency 2200 MHz



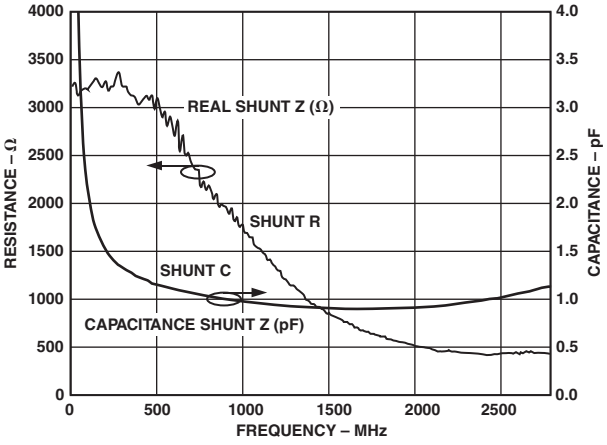
TPC 44. Phase Output vs. Input Phase Difference, $P_{INPA} = P_{INPB}$, $P_{INPA} = P_{INPB}$ + 10 dB, $P_{INPA} = P_{INPB}$ – 10 dB, Frequency 1900 MHz, Supply 5 V



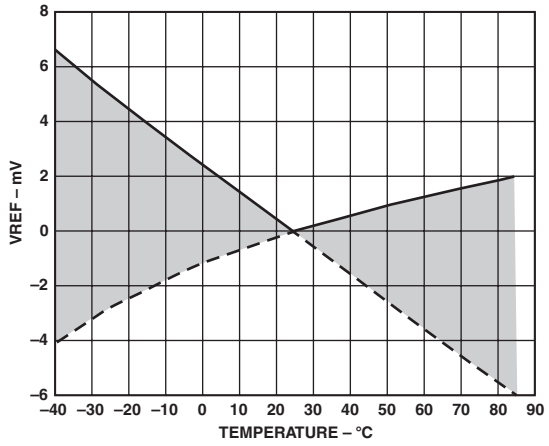
TPC 47. Phase Output Instantaneous Slope, $P_{INPA} = P_{INPB}$, $P_{INPA} = P_{INPB}$ + 10 dB, $P_{INPA} = P_{INPB}$ – 10 dB, Frequency 2200 MHz



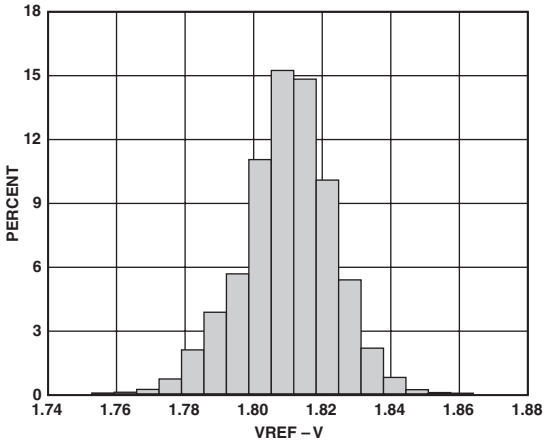
TPC 45. Phase Output Instantaneous Slope, $P_{INPA} = P_{INPB}$, $P_{INPA} = P_{INPB}$ + 10 dB, $P_{INPA} = P_{INPB}$ – 10 dB, Frequency 1900 MHz, Supply 5 V



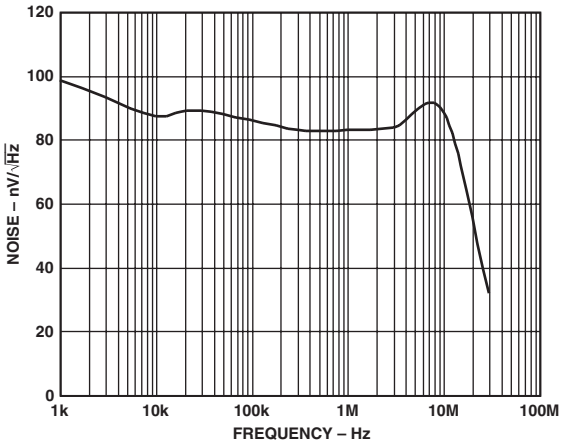
TPC 48. Input Impedance, Modeled as Shunt R in Parallel with Shunt C



TPC 49. Change in VREF vs. Temperature, Three Sigma to Either Side of Mean



TPC 51. VREF Distribution, 17,000 Units



TPC 50. VREF Output Noise Spectral Density vs. Frequency

GENERAL DESCRIPTION AND THEORY

The AD8302 measures the magnitude ratio, defined here as gain, and phase difference between two signals. A pair of matched logarithmic amplifiers provide the measurement, and their hard-limited outputs drive the phase detector.

Basic Theory

Logarithmic amplifiers (log amps) provide a logarithmic compression function that converts a large range of input signal levels to a compact decibel-scaled output. The general mathematical form is:

$$V_{OUT} = V_{SLP} \log\left(V_{IN} / V_Z\right) \quad (1)$$

where V_{IN} is the input voltage, V_Z is called the intercept (voltage), and V_{SLP} is called the slope (voltage). It is assumed throughout that log(x) represents the log10(x) function. V_{SLP} is thus the volts/decade, and since a decade of voltage corresponds to 20 dB, V_{SLP}/20 is the volts/dB. V_Z is the value of input signal that results in an output of zero and need not correspond to a physically realizable part of the log amp signal range. While the slope is fundamentally a characteristic of the log amp, the intercept is a function of the input waveform as well.[1] Furthermore, the intercept is typically more sensitive to temperature and frequency than the slope. When single log amps are used for power measurement, this variability introduces errors into the absolute accuracy of the measurement since the intercept represents a reference level.

The AD8302 takes the difference in the output of two identical log amps, each driven by signals of similar waveforms but at different levels. Since subtraction in the logarithmic domain corresponds to a ratio in the linear domain, the resulting output becomes:

$$V_{MAG} = V_{SLP} \log\left(V_{INA} / V_{INB}\right) \quad (2)$$

where V_{INA} and V_{INB} are the input voltages, V_{MAG} is the output corresponding to the magnitude of the signal level difference, and V_{SLP} is the slope. Note that the intercept, V_Z, has dropped out. Unlike the measurement of power, when measuring a dimensionless quantity such as relative signal level, no independent reference or intercept need be invoked. In essence, one signal serves as the intercept for the other. Variations in intercept due to frequency, process, temperature, and supply voltage affect both channels identically and hence do not affect the difference. This technique depends on the two log amps being well matched in slope and intercept to ensure cancellation. This is the case for an integrated pair of log amps. Note that if the two signals have different waveforms (e.g., different peak-to-average ratios) or different frequencies, an intercept difference may appear, introducing a systematic offset.

The log amp structure consists of a cascade of linear/limiting gain stages with demodulating detectors. Further details about the structure and function of log amps can be found in data sheets for other log amps produced by Analog Devices.[2] The output of the final stage of a log amp is a fully limited signal over most of the input dynamic range. The limited outputs from both log amps drive an exclusive-OR style digital phase detector. Operating strictly on the relative zero-crossings of the limited signals, the extracted phase difference is independent of the original input signal levels. The phase output has the general form:

$$V_{PHS} = V_\Phi \left[\Phi\left(V_{INA}\right) - \Phi\left(V_{INB}\right)\right] \quad (3)$$

where V_Φ is the phase slope in mV/degree and Φ is each signal's relative phase in degrees.

Structure

The general form of the AD8302 is shown in Figure 2. The major blocks consist of two demodulating log amps, a phase detector, output amplifiers, a biasing cell, and an output reference voltage buffer. The log amps and phase detector process the high frequency signals and deliver the gain and phase information in current form to the output amplifiers. The output amplifiers determine the final gain and phase scaling. External filter capacitors set the averaging time constants for the respective outputs. The reference buffer provides a 1.80 V reference voltage that tracks the internal scaling constants.

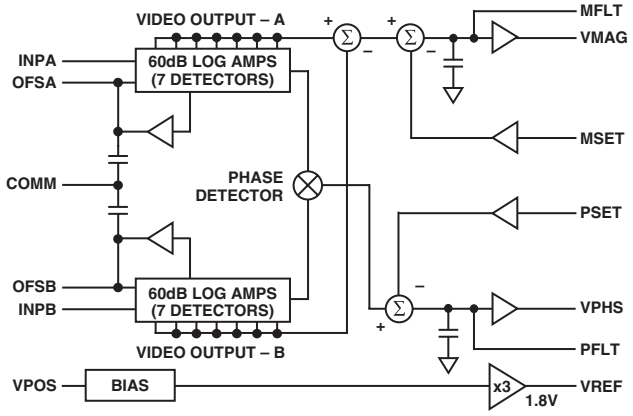


Figure 2. General Structure

Each log amp consists of a cascade of six 10 dB gain stages with seven associated detectors. The individual gain stages have 3 dB bandwidths in excess of 5 GHz. The signal path is fully differential to minimize the effect of common-mode signals and noise. Since there is a total of 60 dB of cascaded gain, slight dc offsets can cause limiting of the latter stages, which may cause measurement errors for small signals. This is corrected by a feedback loop. The nominal high-pass corner frequency, f_{HP}, of this loop is set internally at 200 MHz but can be lowered by adding external capacitance to the OFSA and OFSB pins. Signals at frequencies well below the high-pass corner are indistinguishable from dc offsets and are also nulled. The difference in the log amp outputs is performed in the current domain, yielding by analogy to Equation 2:

$$I_{LA} = I_{SLP} \log\left(V_{INA} / V_{INB}\right) \quad (4)$$

where I_{LA} and I_{SLP} are the output current difference and the characteristic slope (current) of the log amps, respectively. The slope is derived from an accurate reference designed to be insensitive to temperature and supply voltage.

The phase detector uses a fully symmetric structure with respect to its two inputs to maintain balanced delays along both signal paths. Fully differential signaling again minimizes the sensitivity to common-mode perturbations. The current-mode equivalent to Equation 3 is:

$$I_{PD} = I_\Phi \left[\Phi\left(V_{INA}\right) - \Phi\left(V_{INB}\right) - 90°\right] \quad (5)$$

where I_{PD} and I_Φ are the output current and characteristic slope associated with the phase detector, respectively. The slope is derived from the same reference as the log amp slope.

NOTES

[1]See the data sheet for the AD640 for a description of the effect of waveform on the intercept of log amps.

[2]For example, see the data sheet for the AD8307.

Note that by convention, the phase difference is taken in the range from –180° to +180°. Since this style of phase detector does not distinguish between ±90°, it is considered to have an unambiguous 180° phase difference range that can be either 0° to +180° centered at +90° or 0° to –180° centered at –90°.

The basic structure of both output interfaces is shown in Figure 3. It accepts a setpoint input and includes an internal integrating/averaging capacitor and a buffer amplifier with gain K. External access to these setpoints provides for several modes of operation and enables flexible tailoring of the gain and phase transfer characteristics. The setpoint interface block, characterized by a transresistance R_F, generates a current proportional to the voltage presented to its input pin, MSET or PSET. A precise offset voltage of 900 mV is introduced internally to establish the center-point (V_{CP}) for the gain and phase functions, i.e., the setpoint voltage that corresponds to a gain of 0 dB and a phase difference of 90°. This setpoint current is subtracted from the signal current, I_{IN}, coming from the log amps in the gain channel or from the phase detector in the phase channel. The resulting difference is integrated on the averaging capacitors at either pin MFLT or PFLT and then buffered by the output amplifier to the respective output pins, VMAG and VPHS. With this open-loop arrangement, the output voltage is a simple integration of the difference between the measured gain/phase and the desired setpoint:

$$V_{OUT} = R_F\left(I_{IN} - I_{FB}\right) / \left(sT\right) \tag{6}$$

where I_{FB} is the feedback current equal to $(V_{SET} - V_{CP})/R_F$, V_{SET} is the setpoint input, and T is the integration time constant equal to $R_F C_{AVE}/K$, where C_{AVE} is the parallel combination of the internal 1.5 pF and the external capacitor C_{FLT}.

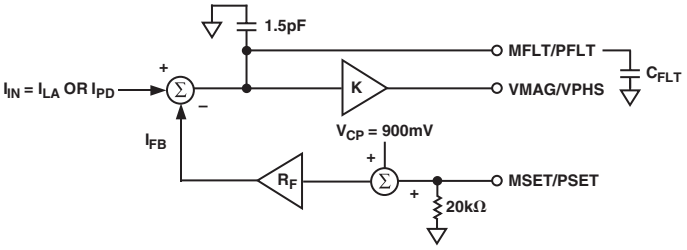


Figure 3. Simplified Block Diagram of the Output Interface

BASIC CONNECTIONS

Measurement Mode

The basic function of the AD8302 is the direct measurement of gain and phase. When the output pins, VMAG and VPHS, are connected directly to the feedback setpoint input pins, MSET and PSET, the default slopes and center points are invoked. This basic connection shown in Figure 4 is termed the measurement mode. The current from the setpoint interface is forced by the integrator to be equal to the signal currents coming from the log amps and phase detector. The closed loop transfer function is thus given by:

$$V_{OUT} = \left(I_{IN} R_F + V_{CP}\right) / \left(1 + sT\right) \tag{7}$$

The time constant T represents the single-pole response to the envelope of the dB-scaled gain and the degree-scaled phase functions. A small internal capacitor sets the maximum envelope bandwidth to approximately 30 MHz. If no external C_{FLT} is used, the AD8302 can follow the gain and phase envelopes within this bandwidth. If longer averaging is desired, C_{FLT} can be added as necessary according to T (ns) = 3.3 × C_{AVE} (pF). For best transient response with minimal overshoot, it is recommended that 1 pF minimum value external capacitors be added to the MFLT and PFLT pins.

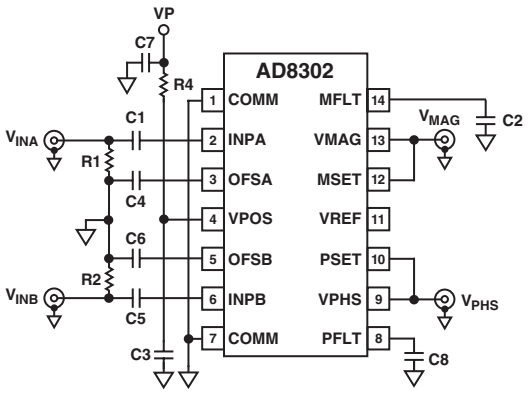


Figure 4. Basic Connections in Measurement Mode with 30 mV/dB and 10 mV/Degree Scaling

In the low frequency limit, the gain and phase transfer functions given in Equations 4 and 5 become:

$$V_{MAG} = R_F I_{SLP} \log\left(V_{INA} / V_{INB}\right) + V_{CP} \text{ or} \tag{8a}$$

$$V_{MAG} = \left(R_F I_{SLP} / 20\right)\left(P_{INA} - P_{INB}\right) + V_{CP} \tag{8b}$$

$$V_{PHS} = -R_F I_\Phi \left(\left|\Phi\left(V_{INA}\right) - \Phi\left(V_{INB}\right)\right| - 90°\right) + V_{CP} \tag{9}$$

which are illustrated in Figure 5. In Equation 8b, P_{INA} and P_{INB} are the power in dBm equivalent to V_{INA} and V_{INB} at a specified reference impedance. For the gain function, the slope represented by $R_F I_{SLP}$ is 600 mV/decade or, dividing by 20 dB/decade, 30 mV/dB. With a center point of 900 mV for 0 dB gain, a range of –30 dB to +30 dB covers the full-scale swing from 0 V to 1.8 V. For the phase function, the slope represented by $R_F I_\Phi$ is 10 mV/degree. With a center point of 900 mV for 90°, a range of 0° to 180° covers the full-scale swing from 1.8 V to 0 V. The range of 0° to –180° covers the same full-scale swing but with the opposite slope.

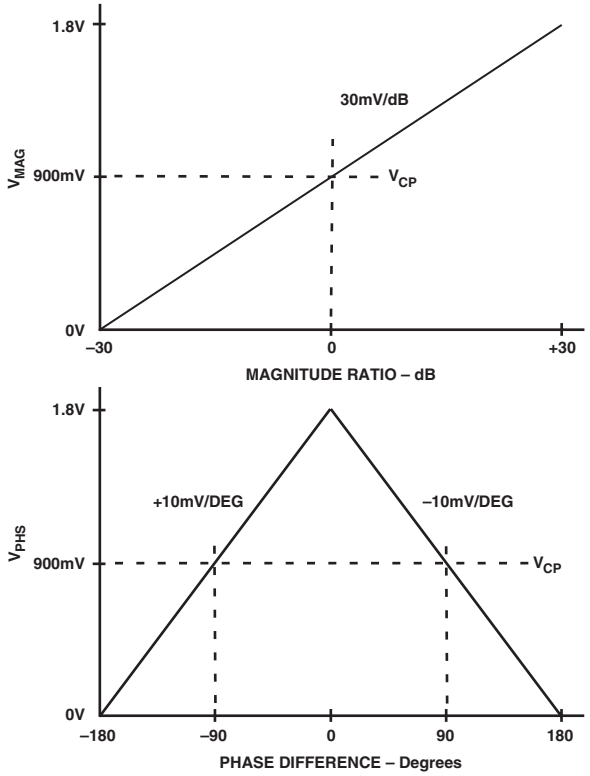


Figure 5. Idealized Transfer Characteristics for the Gain and Phase Measurement Mode

Interfacing to the Input Channels

The single-ended input interfaces for both channels are identical. Each consists of a driving pin, INPA and INPB, and an ac-grounding pin, OFSA and OFSB. All four pins are internally dc-biased at about 100 mV from the positive supply and should be externally ac-coupled to the input signals and to ground. For the signal pins, the coupling capacitor should offer negligible impedance at the signal frequency. For the grounding pins, the coupling capacitor has two functions: It provides ac grounding and sets the high-pass corner frequency for the internal offset compensation loop. There is an internal 10 pF capacitor to ground that sets the maximum corner to approximately 200 MHz. The corner can be lowered according the formula f_{HP} (MHz) = $2/C_C$(nF), where C_C is the total capacitance from OFSA or OFSB to ground, including the internal 10 pF.

The input impedance to INPA and INPB is a function of frequency, the offset compensation capacitor, and package parasitics. At moderate frequencies above f_{HP}, the input network can be approximated by a shunt 3 kΩ resistor in parallel with a 2 pF capacitor. At higher frequencies, the shunt resistance decreases to approximately 500 Ω. The Smith Chart in Figure 6 shows the input impedance over the frequency range 100 MHz to 3 GHz.

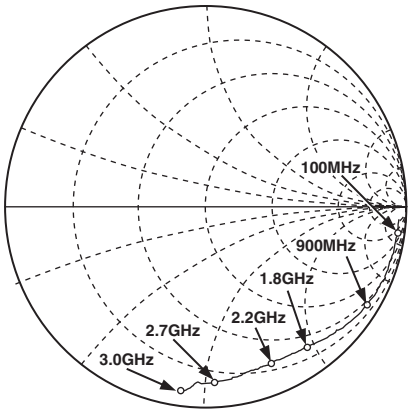


Figure 6. Smith Chart Showing the Input Impedance of a Single Channel from 100 MHz to 3 GHz

A broadband resistive termination on the signal side of the coupling capacitors can be used to match to a given source impedance. The value of the termination resistor, R_T, is determined by:

$$R_T = R_{IN}R_S / \left(R_{IN} - R_S\right) \quad (10)$$

where R_{IN} is the input resistance and R_S the source impedance. At higher frequencies, a reactive, narrow-band match might be desirable to tune out the reactive portion of the input impedance. An important attribute of the two-log-amp architecture is that if both channels are at the same frequency and have the same input network, then impedance mismatches and reflection losses become essentially common-mode and hence do not impact the relative gain and phase measurement. However, mismatches in these external components can result in measurement errors.

Dynamic Range

The maximum measurement range for the gain subsystem is limited to a total of 60 dB distributed from –30 dB to +30 dB. This means that both gain and attenuation can be measured. The limits are determined by the minimum and maximum levels that each individual log amp can detect. In the AD8302, each log amp can detect inputs ranging from –73 dBV [(223 μV, –60 dBm re: 50 Ω to –13 dBV (223 mV, 0 dBm re: 50 Ω)]. Note that log amps respond to voltages and not power. An equivalent power can be inferred given an impedance level, e.g., to convert from dBV to dBm in a 50 Ω system, simply add 13 dB. To cover the entire range, it is necessary to apply a reference level to one log amp that corresponds precisely to its midrange. In the AD8302, this level is at –43 dBV, which corresponds to –30 dBm in a 50 Ω environment. The other channel can now sweep from its low end, 30 dB below midrange, to its high end, 30 dB above midrange. If the reference is displaced from midrange, some measurement range will be lost at the extremes. This can occur either if the log amps run out of range or if the rails at ground or 1.8 V are reached. Figure 7 illustrates the effect of the reference channel level placement. If the reference is chosen lower than midrange by 10 dB, then the lower limit will be at –20 dB rather than –30 dB. If the reference chosen is higher by 10 dB, the upper limit will be 20 dB rather than 30 dB.

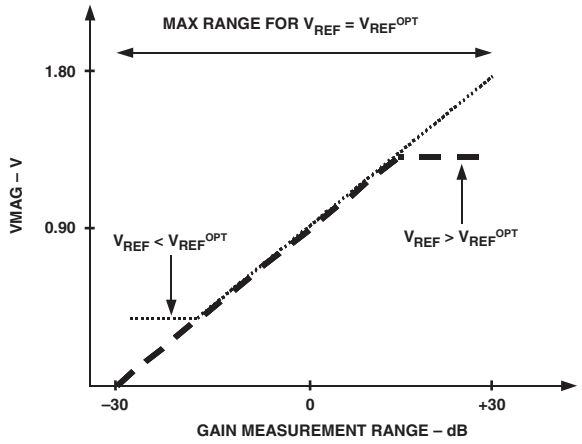


Figure 7. The Effect of Offsetting the Reference Level Is to Reduce the Maximum Dynamic Range

The phase measurement range is of 0° to 180°. For phase differences of 0° to –180°, the transfer characteristics are mirrored as shown in Figure 5, with a slope of the opposite sign. The phase detector responds to the relative position of the zero crossings between the two input channels. At higher frequencies, the finite rise and fall times of the amplitude limited inputs create an ambiguous situation that leads to inaccessible dead zones at the 0° and 180° limits. For maximum phase difference coverage, the reference phase difference should be set to 90°.

Cross Modulation of Magnitude and Phase

At high frequencies, unintentional cross coupling between signals in Channels A and B inevitably occurs due to on-chip and board-level parasitics. When the two signals presented to the AD8302 inputs are at very different levels, the cross coupling introduces cross modulation of the phase and magnitude responses. If the two signals are held at the same relative levels and the phase between them is modulated then only the phase output should respond. Due to phase-to-amplitude cross modulation, the magnitude output shows a residual response. A similar effect occurs when the relative phase is held constant while the magnitude difference is modulated, i.e., an expected magnitude response and a residual phase response are observed due to amplitude-to-phase cross modulation. The point where these effects are noticeable depends on the signal frequency and the magnitude of the difference. Typically, for differences <20 dB, the effects of cross modulation are negligible at 900 MHz.

Modifying the Slope and Center Point

The default slope and center point values can be modified with the addition of external resistors. Since the output interface blocks are generalized for both magnitude and phase functions, the scaling modification techniques are equally valid for both outputs. Figure 8 demonstrates how a simple voltage divider from the VMAG and VPHS pins to the MSET and PSET pins can be used to modify the slope. The increase in slope is given by 1 + R1/(R2‖20 kΩ). Note that it may be necessary to account for the MSET and PSET input impedance of 20 kΩ which has a ±20% manufacturing tolerance. As is generally true in such feedback systems, envelope bandwidth is decreased and the output noise transferred from the input is increased by the same factor. For example, by selecting R1 and R2 to be 10 kΩ and 20 kΩ, respectively, gain slope increases from the nominal 30 mV/dB by a factor of 2 to 60 mV/dB. The range is reduced by a factor of 2 and the new center point is at –15 dB, i.e., the range now extends from –30 dB, corresponding to V_{MAG} = 0 V, to 0 dB, corresponding to V_{MAG} = 1.8 V.

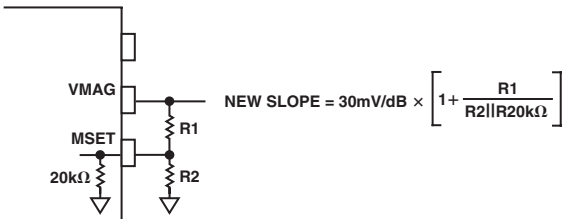


Figure 8. Increasing the Slope Requires the Inclusion of a Voltage Divider

Repositioning the center point back to its original value of 0 dB simply requires that an appropriate voltage be applied to the grounded side of the lower resistor in the voltage divider. This voltage may be provided externally or derived from the internal reference voltage on pin VREF. For the specific choice of R2 = 20 kΩ, the center point is easily readjusted to 0 dB by connecting the VREF pin directly to the lower pin of R2 as shown in Figure 9. The increase in slope is now simplified to 1 + R1/10 kΩ. Since this 1.80 V reference voltage is derived from the same band gap reference that determines the nominal center point, their tracking with temperature, supply, and part-to-part variations should be better in comparison to a fixed external voltage. If the center point is shifted to 0 dB in the previous example where the slope was doubled, then the range spans from –15 dB at V_{MAG} = 0 V to 15 dB at V_{MAG} = 1.8 V.

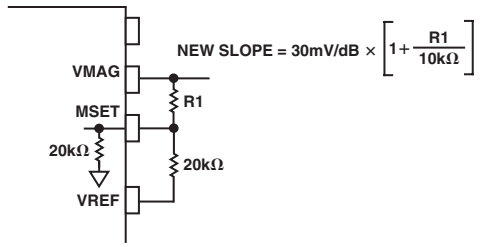


Figure 9. The Center Point Is Repositioned with the Help of the Internal Reference Voltage of 1.80 V

Comparator and Controller Modes

The AD8302 can also operate in a comparator mode if used in the arrangement shown in Figure 10 where the DUT is the element to be evaluated. The VMAG and VPHS pins are no longer connected to MSET and PSET. The trip-point thresholds for the gain and phase difference comparison are determined by the voltages applied to pins MSET and PSET according to:

$$V_{MSET}(V) = 30\ mV/dB \times Gain^{SP}(dB) + 900\ mV \quad (11)$$

$$V_{PSET}(V) = -10\ mV/^\circ \times \left(|\ Phase^{SP}(^\circ)\ | - 90^\circ \right) + 900\ mV \quad (12)$$

where $Gain^{SP}$ (dB) and $Phase^{SP}$ (°) are the desired gain and phase thresholds. If the actual gain and phase between the two input channels differ from these thresholds, the V_{MAG} and V_{PHS} outputs toggle like comparators, i.e.,

$$V_{MAG} = \begin{cases} 1.8\,V\ if\ Gain > Gain^{SP} \\ 0\,V\ if\ Gain < Gain^{SP} \end{cases} \quad (13)$$

$$V_{PHS} = \begin{cases} 1.8\,V\ if\ Phase > Phase^{SP} \\ 0\,V\ if\ Phase < Phase^{SP} \end{cases} \quad (14)$$

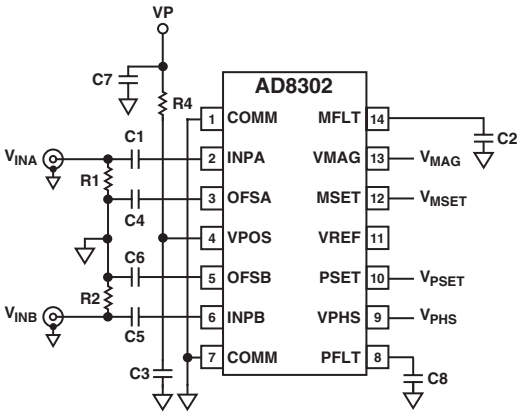


Figure 10. Disconnecting the Feedback to the Setpoint Controls, the AD8302 Operates in Comparator Mode

The comparator mode can be turned into a controller mode by closing the loop around the VMAG and VPHS outputs. Figure 11 illustrates a closed loop controller that stabilizes the gain and phase of a DUT with gain and phase adjustment elements. If VMAG and VPHS are properly conditioned to drive gain and phase adjustment blocks preceding the DUT, the actual gain and phase of the DUT will be forced toward the prescribed setpoint gain and phase given in Equations 11 and 12. These are essentially AGC and APC loops. Note that as with all control loops of this kind, loop dynamics and appropriate interfaces all must be considered in more detail.

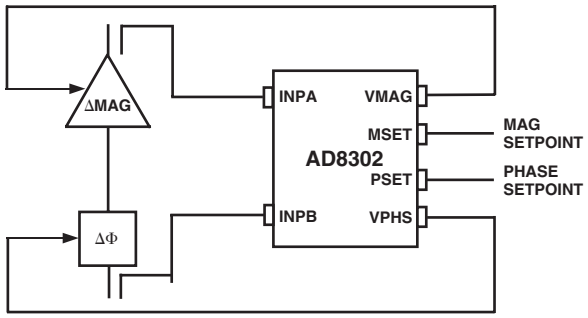


Figure 11. By Applying Overall Feedback to a DUT Via External Gain and Phase Adjusters, the AD8302 Acts as a Controller

APPLICATIONS

Measuring Amplifier Gain and Compression

The most fundamental application of AD8302 is the monitoring of the gain and phase response of a functional circuit block such as an amplifier or a mixer. As illustrated in Figure 12, directional couplers, DC_B and DC_A, sample the input and output signals of the "Black Box" DUT. The attenuators ensure that the signal levels presented to the AD8302 fall within its dynamic range. From the discussion in the Dynamic Range section, the optimal choice places both channels at P_{OPT} = –30 dBm referenced to 50 Ω, which corresponds to –43 dBV. To achieve this, the combination of coupling factor and attenuation are given by:

$$C_B + L_B = P_{IN} - P_{OPT} \quad (15)$$

$$C_A + L_A = P_{IN} + GAIN_{NOM} - P_{OPT} \quad (16)$$

where C_B and C_A are the coupling coefficients, L_B and L_A are the attenuation factors, and $GAIN_{NOM}$ is the nominal DUT gain. If identical couplers are used for both ports, then the difference in the two attenuators compensates for the nominal DUT gain. When the actual gain is nominal, the VMAG output is 900 mV, corresponding to 0 dB. Variations from nominal gain appear as a deviation from 900 mV or 0 dB with a 30 mV/dB scaling. Depending on the nominal insertion phase associated with DUT, the phase measurement may require a fixed phase shift in series with one of the channels to bring the nominal phase difference presented to the AD8302 near the optimal 90° point.

When the insertion phase is nominal, the VPHS output is 900 mV. Deviations from the nominal are reported with a 10 mV/degree scaling. Table I gives suggested component values for the measurement of an amplifier with a nominal gain of 10 dB and an input power of –10 dBm.

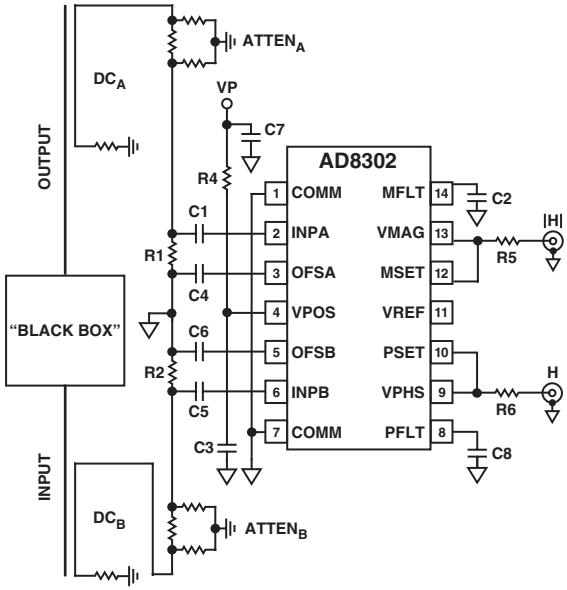


Figure 12. Using the AD8302 to Measure the Gain and Insertion Phase of an Amplifier or Mixer

Table I. Component Values for Measuring a 10 dB Amplifier with an Input Power of –10 dBm

Component	Value	Quantity
R1, R2	52.3 Ω	2
R5, R6	100 Ω	2
C1, C4, C5, C6	0.001 μF	4
C2, C8	Open	
C3	100 pF	1
C7	0.1 μF	1
AttenA	10 dB (See Text)	1
AttenB	1 dB (See Text)	1
DC_A, DC_B	20 dB	2

The gain measurement application can also monitor gain and phase distortion in the form of AM-AM (gain compression) and AM-PM conversion. In this case, the nominal gain and phase corresponds to those at low input signal levels. As the input level is increased, output compression and excess phase shifts are measured as deviations from the low level case. Note that the signal levels over which the input is swept must remain within the dynamic range of the AD8302 for proper operation.

Reflectometer

The AD8302 can be configured to measure the magnitude ratio and phase difference of signals that are incident on and reflected from a load. The vector reflection coefficient, Γ, is defined as,

$$\Gamma = \textit{Reflected Voltage} / \textit{Incident Voltage} = \left(Z_L - Z_O\right) / \left(Z_L + Z_O\right) \quad (17)$$

where Z_L is the complex load impedance and Z_O is the characteristic system impedance.

The measured reflection coefficient can be used to calculate the level of impedance mismatch or standing wave ratio (SWR) of a particular load condition. This proves particularly useful in diagnosing varying load impedances such as antennas that can degrade performance and even cause physical damage. The vector reflectometer arrangement given in Figure 13 consists of a pair of directional couplers that sample the incident and reflected signals. The attenuators reposition the two signal levels within the dynamic range of the AD8302. In analogy to Equations 15 and 16, the attenuation factors and coupling coefficients are given by:

$$C_B + L_B = P_{IN} - P_{OPT} \quad (18)$$

$$C_A + L_A = P_{IN} + \Gamma_{NOM} - P_{OPT} \quad (19)$$

where Γ_{NOM} is the nominal reflection coefficient in dB and is negative for passive loads. Consider the case where the incident signal is 10 dBm and the nominal reflection coefficient is –19 dB. As shown in Figure 13, using 20 dB couplers on both sides and –30 dBm for P_{OPT}, the attenuators for Channel A and B paths are 1 dB and 20 dB, respectively. The magnitude and phase of the reflection coefficient are available at the VMAG and VPHS pins scaled to 30 mV/dB and 10 mV/degree. When Γ is –19 dB, the VMAG output is 900 mV.

The measurement accuracy can be compromised if board level details are not addressed. Minimize the physical distance between the series connected couplers since the extra path length adds phase error to Γ. Keep the paths from the couplers to the AD8302 as well matched as possible since any differences introduce measurement errors. The finite directivity, D, of the couplers sets the minimum detectable reflection coefficient, i.e., $|\Gamma_{MIN}(\text{dB})| < |\text{D}(\text{dB})|$.

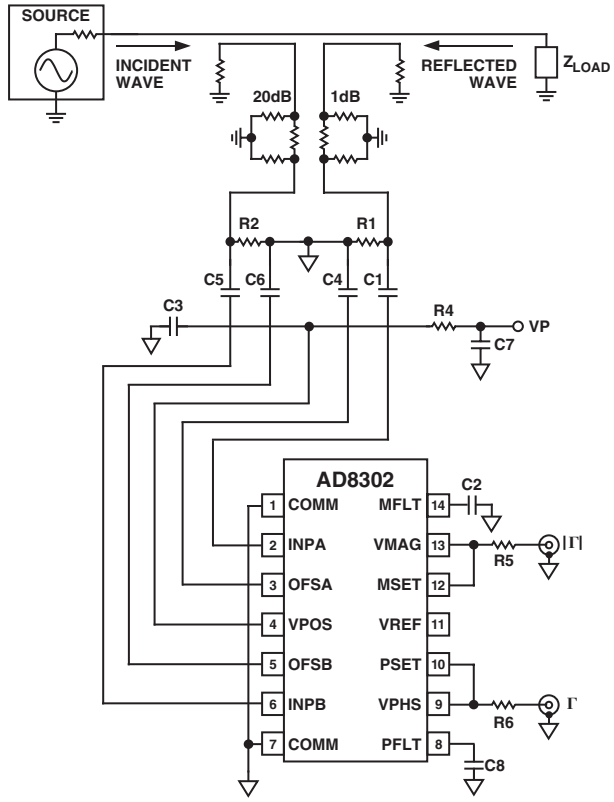


Figure 13. Using the AD8302 to Measure the Vector Reflection Coefficient Off an Arbitrary Load

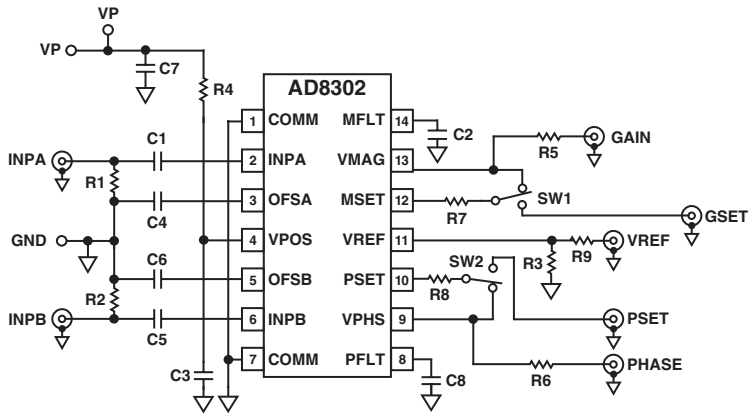


Figure 14. Evaluation Board Schematic

Table II. P1 Pin Allocations

1	Common
2	VPOS
3	Common

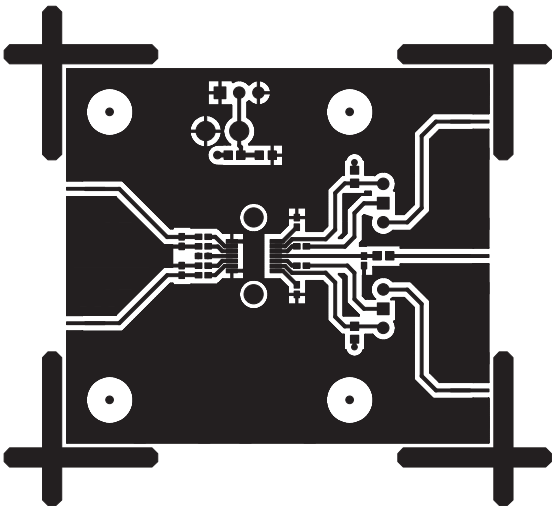


Figure 15a. Component Side Metal of Evaluation Board

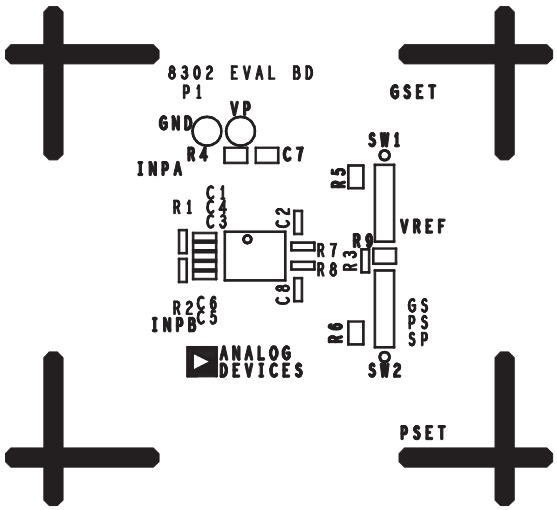


Figure 15b. Component Side Silkscreen of Evaluation Board

Table III. Evaluation Board Configuration Options

Component	Function	Default Condition
P1	Power Supply and Ground Connector: Pin 2 VPOS and Pins 1 and 3 Ground.	Not Applicable
R1, R2	Input Termination. Provide termination for input sources.	R1 = R2 = 52.3 Ω (Size 0402)
R3	VREF Output Load. This load is optional and is meant to allow the user to simulate their circuit loading of the device.	R3 = 1 kΩ (Size 0603)
R5, R6, R9	Snubbing Resistor	R5 = R6 = 0 Ω (Size 0603) R9 = 0 Ω (Size 0603)
C3, C7, R4	Supply Decoupling	C3 = 100 pF (Size 0603) C7 = 0.1 µF (Size 0603) R4 = 0 Ω (Size 0603)
C1, C5	Input AC-Coupling Capacitors	C1 = C5 = 1 nF (Size 0603)
C2, C8	Video Filtering. C2 and C8 limit the video bandwidth of the gain and phase output respectively.	C2 = C8 = Open (Size 0603)
C4, C6	Offset Feedback. These set the high-pass corner of the offset cancellation loop and thus with the input ac-coupling capacitors the minimum operating frequency.	C4 = C6 = 1 nF (Size 0603)
SW1	GSET Signal Source. When SW1 is in the position shown, the device is in gain measure mode; when switched, it operates in comparator mode and a signal must be applied to GSET.	SW1 = Installed
SW2	PSET Signal Source. When SW2 is in the position shown, the device is in phase measure mode; when switched, it operates in comparator mode and a signal must be applied to PSET.	SW1 = Installed

CHARACTERIZATION SETUPS AND METHODS

The general hardware configuration used for most of the AD8302 characterization is shown in Figure 16. The characterization board is similar to the Customer Evaluation Board. Two reference-locked R and S SMT03 signal generators are used as the inputs to INPA and INPB, while the gain and phase outputs are monitored using both a TDS 744A oscilloscope with 10× high impedance probes and Agilent 34401A multimeters.

Gain

The basic technique used to evaluate the static gain (VMAG) performance was to set one source to a fixed level and sweep the amplitude of the other source, while measuring the VMAG output with the DMM. In practice, the two sources were run at 100 kHz frequency offset and average output measured with the DMM to alleviate errors that might be induced by gain/phase modulation due to phase jitter between the two sources.

The errors stated are the difference between a best fit line calculated by a linear regression and the actual measured data divided by the slope of the line to give an error in V/dB. The referred to 25°C error uses this same method while always using the slope and intercept calculated for that device at 25°C.

Response measurement made of the VMAG output used the configuration shown in Figure 17. The variable attenuator, Alpha AD260, is driven with a HP8112A pulse generator producing a change in RF level within 10 ns.

Noise spectral density measurements were made using a HP3589A with the inputs delivered through a Narda 4032C 90° phase splitter.

To measure the modulation of VMAG due to phase variation again the sources were run at a frequency offset, f_{OS}, effectively creating a continuous linear change in phase going through 360° once every $1/f_{OS}$ seconds. The VMAG output is then measured with a DSO. When perceivable, only at high frequencies and large input magnitude differences, the linearly ramping phase creates a near sinusoid output riding on the expected VMAG dc output level. The curves in TPC 24 show the peak-to-peak output level measured with averaging.

Phase

The majority of the VPHS output data was collected by generating phase change, again by operating the two input sources with a small frequency offset (normally 100 kHz) using the same configuration shown in Figure 16. Although this method gives excellent linear phase change, good for measurement of slope and linearity, it lacks an absolute phase reference point. In the curves showing swept phase, the phase at which the VPHS is the same as VPHS with no input signal is taken to be –90° and all other angles are references to there. Typical Performance Curves show two figures of merit; instantaneous slope and error. Instantaneous slope, as shown in TPCs 43, 44, 45, and 47, was calculated simply by taking the delta in VPHS over angular change for adjacent measurement points.

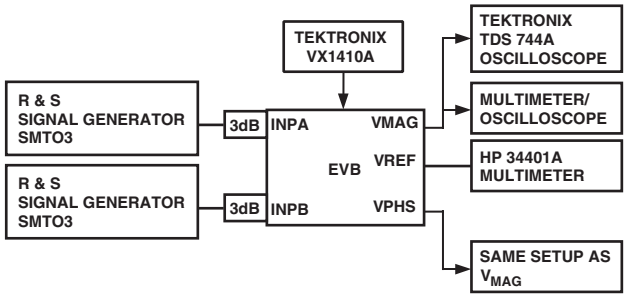


Figure 16. Primary Characterization Setup

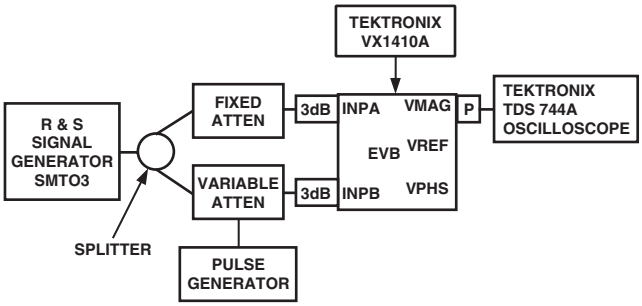
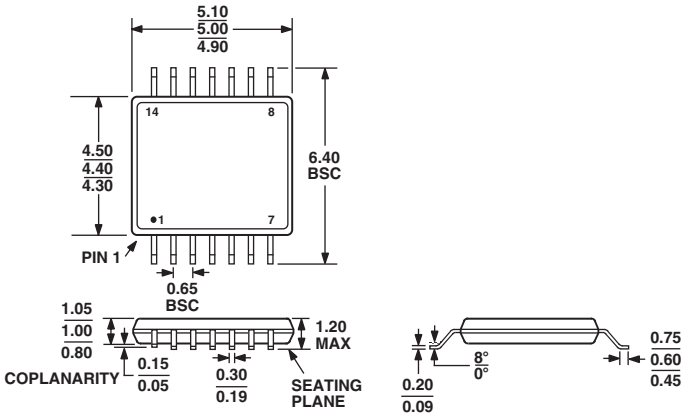


Figure 17. VMAG Dynamic Performance Measurement Setup

OUTLINE DIMENSIONS

14-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-14)

Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-153AB-1

Revision History

Location	Page
7/02—Data Sheet changed from REV. 0 to REV. A.	
TPCs 3 through 6 replaced	6

C02492–0–7/02(A)

PRINTED IN U.S.A.