ORA Technical Report

SKA ADU Board ver. 1.0 Performance Measurements

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LIST OF ABBREVIATIONS

AADC	Aperture Array Design and construction Consortium
AAVS	Aperture Array Verification System
ADC	Analog to Digital Converter
ADI	Analog Devices Incorporation
ADU	Analog to Digital Unit
CPLD	Complex Programmable Logic Device
DGA	Digital Gain Amplifier
DUT	Device Under Test
EMI	Electro Magnetic Interference
ENOB	Effective Number of Bits
FFT	Fast Fourier Transform
FPGA	Field Programmable Gate Array
HW	Hardware
HD	Harmonic Distortion
IIP3	Input Third-Order Intercept Point
IMD	Intermodulation Distortion
LFAA	Low Frequency Aperture Array
LNA	Low Noise Amplifier
LMC	Local monitoring and Control
OIP3	Output Third-Order Intercept Point
PCB	Printed Circuit Board
PLL	Phase Locked Loop
RF	Radio Frequency
RFI	Radio Frequency Interference
RFoF	Radio Frequency signal over Fibre
SFDR	Spurious Free Dynamic Range
SINAD	Signal to Noise and Distortion ratio
SKA	Square Kilometre Array
SKA-LOW	SKA low frequency part of the full telescope
SKAO	SKA Office
SNR	Signal to Noise Ratio
SNRFS	Signal to Noise Ratio referenced to Full Scale
SPI	Serial Peripheral Interface
SW	Software
THD	Total Harmonic Distortion
TPM	Tile Processor Module
UDP	User Datagram Protocol
WDM	Wavelength Division Multiplexing

1 Introduction

This document describes the test campaign carried out at the Medicina Radio Astronomical Station (INAF) for the characterization and evaluation of performances of the Analog to Digital Unit (ADU) Board that is part of the Italian Tile Processing Module (iTPM). This prototype board is one of the candidate backend for SKA-LFAA for first stage channelization and beamforming purposes. The design of the board has been funded by the TECNO PRIN INAF 2013 (technological national research program) under the leadership of Francesco Schillirò (INAF - Catania Observatory).

1.1 Content of the document

The report is organized as follows: in Chapter 2 the board is shortly presented with its main features. Chapter 3 is focused on the performance parameters to be evaluated and on the test methods used to calculate them. A description of the hardware test setup is provided along with some notes about the preparation of the suitable test condition. Chapter 4 deals with the on board firmware and the software scripts to manage the ADU board and to control the instruments of the measurement chain. The principal aspects of the data analysis software for the performance evaluation are reported in Chapter 5 as well as the results of the tests. In Chapter 6 there are the conclusions and some final considerations.

1.2 Scope of the tests

The tests are focused on the performance evaluation of the analogue network before the ADC device installed on the TPM ADU Board, its interconnections with the processing sub-system of the board and the ADC itself. These tests are important also to evaluate the influence of clock distribution circuit.

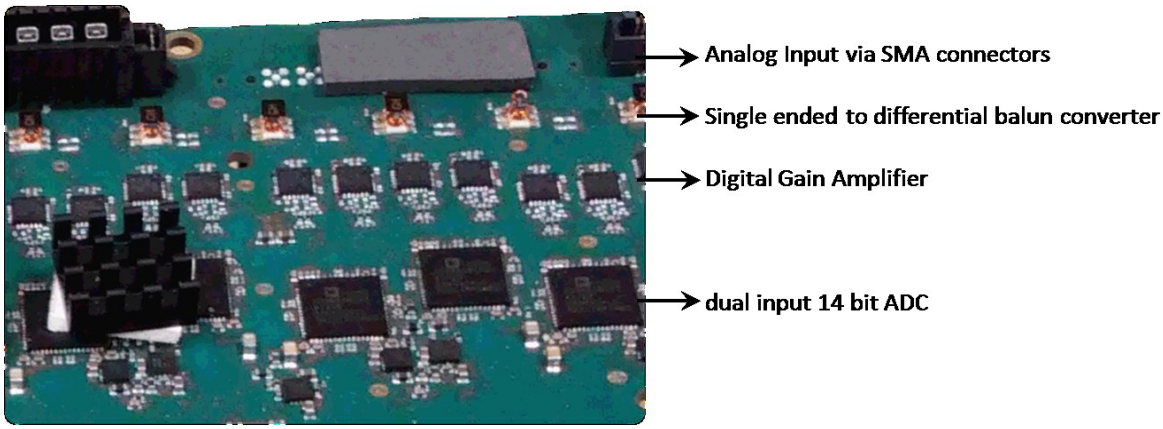


Figure 1: Analogue network and ADC of the ADU board under test.

Figure 1 is a zoomed picture of the tested section of ADU board. From top to bottom, the 32 analog input signals coming from the pre-ADU boards are converted from single ended to differential signals by a balun, amplified by programmable ADA chips and digitized with 14 bit dual-input ADCs that send the 8 most significant bits to the FPGA via high speed links for processing.
The proximity of PCB traces may generate cross talks between input channels, especially in a so dense board, and the unshielded windings of wire coils of the balun may catch external interference signal as an antenna. The aim of tests is also to quantify these undesired effects.

2 iTPM

The Italian Tile Processing Module (iTPM) is the Italian project for the main processing component within the SKA-LFAA element. It is an hybrid analog/digital module that receives 32 analog input signals coming from 16 dual polarization antennas (one SKA tile) via RFoF links (Perini, Rusticelli, Monari, & Schiaffino, 2015) and contributes with the cooperation of other tile processors to form the station beam. In fact, since each iTPM computes the beam of one tile and sums the incoming partial beam from previous tile processors with the tile beam formed locally, when connecting more tile processors in a daisy chain the output of the last will be the beam of the station.
The iTPM is mainly composed of three boards: two pre-ADU boards and one ADU (Analog to Digital Unit) board (Figure 2). The Pre-ADU is devoted to optical-electrical conversion, filtering, amplification and equalization of 32 analog signals. The ADU board has the task of: analog to digital conversion, polyphase filtering, application of calibration and beamforming coefficients, sum of all 32 signals to form the tile beam (local), sum the tile beam with the incoming partial station beam and transmission of the data to the network (switch). More details about the requirements and the design of the signal processing architecture of the ADU board are reported in (Adami, 2015).

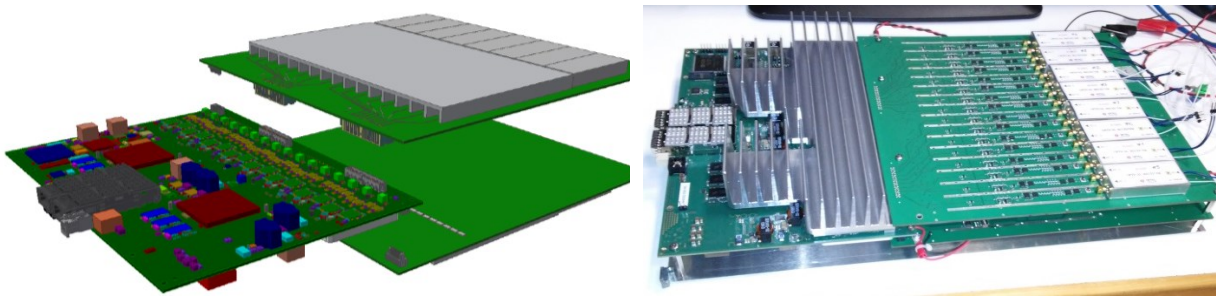


Figure 2: Exploded view drawing of iTPM obtained with 3D CAD (left) and picture of fully assembled module (right).

2.1 Pre-ADU Board

The pre-ADU boards manage 16 input signals each and they are connected to the ADU board one opposite to the other one: one to the ADU top layer and the second one to the ADU bottom layer. It takes in input analog optical signals, converts them in electrical signals and conditions the levels for the ADC dynamic.

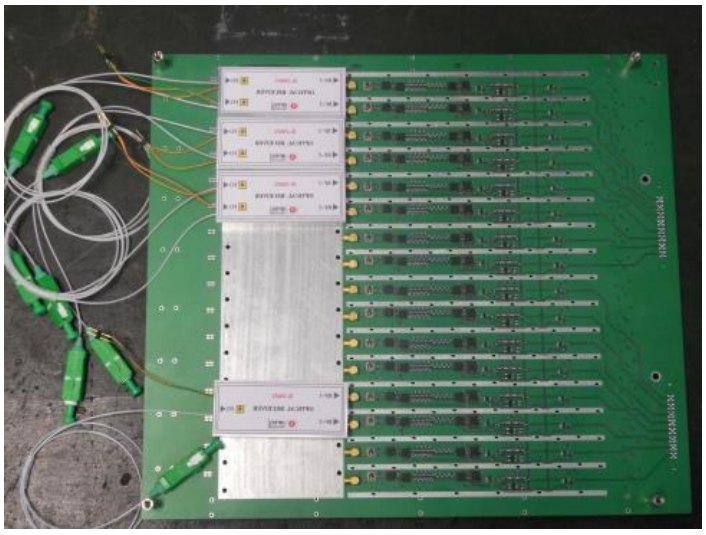


Figure 3: Pre-ADU board.

Detailed documentation of the Pre-ADU board is provided by (Monari, Perini, & Razavi Ghods, 2015) and (Monari, Perini, & Rusticelli, 2015).

2.2 ADU Board

The ADU is the Tile Processor Board of the Square Kilometer Array. It is a 32 channel 1 GHz 8 bit Analog to Digital conversion/preprocessing board, equipped with management functions to support the integration into the rack structure.
State of the art 14 bit AD converter, latest generation 20 nm FPGA and 40 Gbit/s Ethernet optical links have been selected focusing on the best commercial compromise between quality, performance and power consumption.
Compact board size, low noise clock network, advanced 14 layer board build-up, complete Ethernet based management features (including health monitoring capability), high efficiency and low noise power distribution system complete the main board features.
The ADU provides also external synchronization signals and high speed DDR3 memory banks to allow RAW data buffering.
An on-board 32 bit microprocessor and large flash memories allow high-level management operations including on-line multiple configuration selection and structured communication with infrastructure management applications.
The ADU board is provided with a low-level management firmware to perform board configuration and monitoring through the Ethernet interface exploiting a UDP based protocol.
The following list sums up the remarkable ADU characteristics and features:

- Compact size, 6U format compatible
- Thirty-two analog inputs with high quality and high isolation stackable RF 50 Ohm input connectors
- Thirty-two analog programmable drivers (amplifier/attenuator)
- Sixteen dual channels 14 bit 1GSPS A/D converters
- High quality clock distribution system with full JESD204B Subclass 1 capability on all the inputs, with deterministic latency between the channels and the user configurable low noise PLL
- Two Xilinx Ultrascale XCU40 20 nm FPGA devices dedicated to data processing, pin to pin compatible, implementing the same functionality
- Two DDR3, 96 bit memory banks, 6+6 Gbit total size
- Two 40G Ethernet interfaces (QSFP), one for each FPGA
- High speed internal bus to connect the 2 FPGAs, 25 Gbit/s + 25 Gbit/s bidirectional
- Low-level Ethernet gigabit management interface with instant ON flash based Lattice CPLD
- Complete system monitor interface with power, voltage and temperature monitoring
- On board tree 256Mbit SPI user flash for multiple FPGA configuration options
- Second level management microprocessor (ARM Cortex A8, 32 bit, 240 Mhz) for high level remote control of the board
- Highly efficient multistage Power Distribution system, with configurable start up sequence and selective function related to power control capability.

The board is logically divided in the analog to digital chains very close to the pre-ADU connectors (only 15% of the PCB surface area) and the digital part which hosts devices for data processing, management, DC-DC power supplies and input/output interfaces.
Each FPGA manages 16 data streams (one polarization each) connected via JESD204B links, performs the signal processing and transmits the output using Ethernet UDP packets.

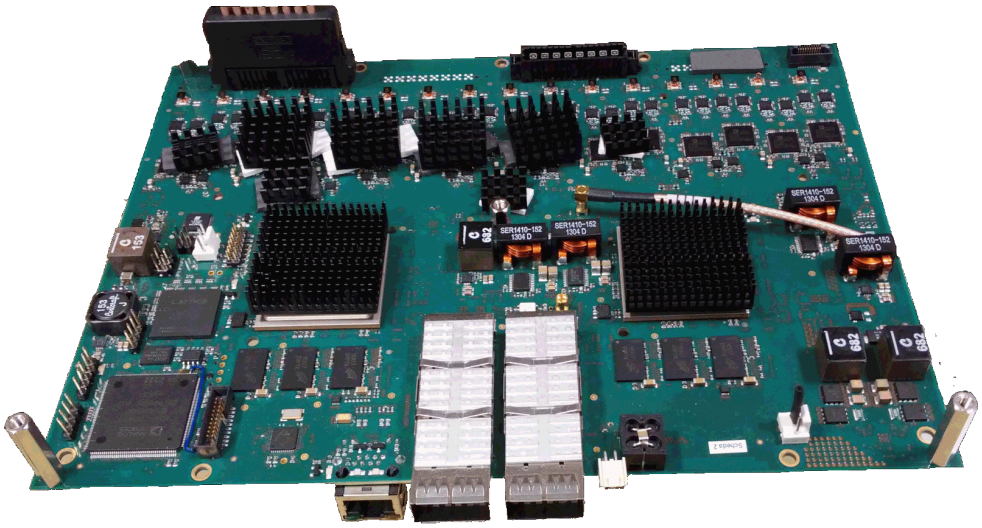


Figure 4: ADU board.

The ADU version 1.0 is the first prototype and two slightly different boards have been initially realized using the same PCB. The only difference between them concerns the presence or absence of a programmable analog signal amplifier in front of the ADC (see next section 2.2.1). Thanks to a resistors and capacitors network the signal paths having the amplifiers can be included or bypassed.
The tests described in this report have been conducted on these two boards for their characterization and performance evaluation.
Further details about the board features can be found in (Pastore, 2015).

2.2.1 ADU Board ver. 1.0: "ADA" and "no ADA" versions

The study for the realization of the analog to digital conversion chain was previously developed in collaboration with the Analog Devices Inc. (ADI). As a result, it has been produced a dual solution using the latest ADC chip technologies (not yet available on the market): a passive matching network (without power amplifier before ADC) and an active matching network (with power amplifier before ADC).
The acronym ADA will be adopted in the document to identify the Analog Devices ADA4961 which is a high performance BiCMOS RF digital gain amplifier (DGA). Having a very low IMD3 it allows converters to achieve their optimum performance with minimal limitations of the driver amplifier. It is optimized for wideband, low distortion performance up to 2 GHz. It has a gain step size of 1 dB with maximum power gain of 18 dB (15 dB of voltage gain) programmable via SPI bus.
The electrical scheme of the active front end with the ADA chip is as follow:

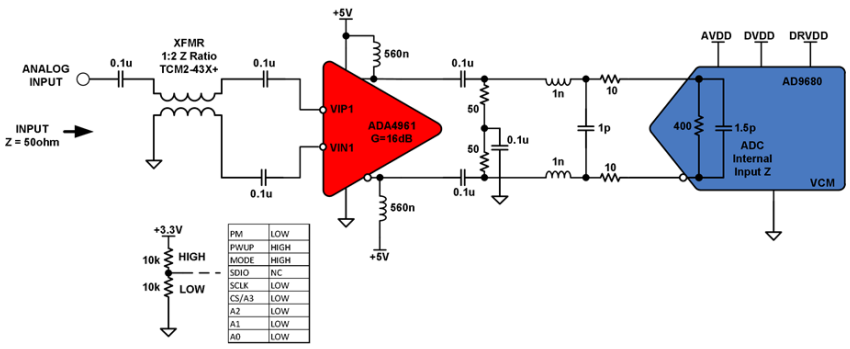


Figure 5: The electrical scheme of the active front end designed for the "ADA" version.

while the passive front end is as follow:

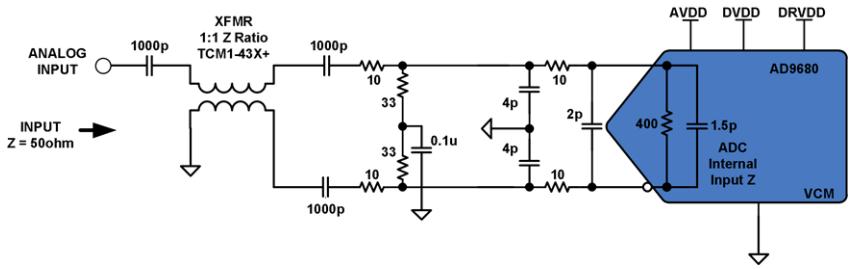


Figure 6: The electrical scheme of the passive front end designed for the "no ADA" version.

2.2.2 ADC

The AD9680 of Analog Devices is a dual, 14-bit, 1 GSPS/500 MSPS analog-to-digital converter (ADC). The device has an on-chip buffer and sample-and-hold circuit designed for low power, small size, and ease of use.

This device is designed for sampling wide bandwidth analog signals of up to 2 GHz. The AD9680 is optimized for wide input bandwidth, high sampling rate, excellent linearity, and low power consumption in a small package.

The dual ADC cores feature a multistage, differential pipelined architecture with integrated output error correction logic. Each ADC features wide bandwidth inputs supporting a variety of user-selectable input ranges. An integrated voltage reference eases design considerations.

The analog input and clock signals are differential inputs. Each ADC data output is internally connected to two digital down-converters (DDCs). Each DDC consists of four cascaded signal processing stages: a 12-bit frequency translator (NCO), and four half-band decimation filters. The DDCs are bypassed by default.

In addition to the DDC blocks, the AD9680 has several functions that simplify the automatic gain control (AGC) function in the communications receiver. The programmable threshold detector allows monitoring of the incoming signal power using the fast detect output bits of the ADC. If the input signal level exceeds the programmable threshold, the fast detect indicator goes high. Because this threshold indicator has low latency, the user can quickly turn down the system gain to avoid an overrange condition at the ADC input.

Users can configure the Subclass 1 JESD204B-based high speed serialized output in a variety of one-, two-, or four-lane configurations, depending on the DDC configuration and the acceptable lane rate of the receiving logic device. Multiple device synchronization is supported through the SYSREF± and SYNCINB± input pins.

The AD9680 has flexible power-down options that allow significant power savings when desired. All of these features can be programmed using a 1.8 V to 3.3 V capable 3-wire SPI.

3 Test definition for ADU board performance evaluation

3.1 Performance parameters

The two ADU boards (with and w/o ADA) have been compared measuring the performance parameters listed in Table 1. Except for Gain Flatness, these are the typical parameters of dynamic (AC) tests used to characterize the A/D converters and they are calculated with FFT analysis.

Performance parameters	
Gain Flatness [dBFS]	The level of the fundamental tone referenced to full scale.
Signal to Noise Ratio [dB]	The ratio of the rms signal amplitude to the rms value of the sum of all spectral components except the first six harmonics and dc.
Signal to Noise Ratio referenced to Full Scale [dBFS]	The ratio of the rms full scale to the rms value of the sum of all spectral components except the first six harmonics and dc.
Spurious Free Dynamic Range [dBc]	The ratio of the rms value of the signal to the rms value of the worst spurious signal (HD or not) regardless of where it falls in the frequency spectrum.
Harmonic Distortion [dBc]	The level of the first six harmonics referenced to the carrier.
Worst Other Spur [dBc]	The level of the worst spurious component excluding the first six harmonically related components referenced to the carrier.
Total Harmonic Distortion [dBc]	The ratio of the rms signal energy to the rms value of the sum of the first six harmonics.
ENOB [bits]	Effective Number of Bits.
Cross-Talk [dBc]	The measure of any feedthrough coupling onto the quiet channel referenced to the carrier.
Second-Order Input Intercept Point [dBm] Third-Order Input Intercept Point [dBm]	$IIPn = P + \frac{\Delta P}{n-1},\ n = 2\ (IIP2),\ 3\ (IIP3)$ where *P* is the output power of the fundamental, and *ΔP* is the difference between *P* and the n^{th}-order Intermodulation Distortion (IMD) product.

Table 1: Performance parameters.

Tests are made with the analog signal at the rated frequency with a signal power of 1 dB below full scale (dBFS) at the input of the ADC.
More details about test procedures and the definition of dynamic performance parameters of ADC can be found in (Arrants, Brannon, & Reeder, 2015), (Kester, 2009) and (Kester, 2005).

3.1.1 FFT analysis

Performance parameters are evaluated with an FFT analysis of the data captured by the board. This analysis, executed by offline data analysis software (see section 5.1), is divided in: single-tone and two-tone FFT analysis depending if only one tone or two tones are injected into ADC input.
It is recommended that frequencies of the input signal are chosen according to the following relation:

$$M * F_i = J * F_s \quad (1)$$

where *M* is the number of samples in the data record, F_i is the frequency of the input signal, *J* is an integer prime number of cycles of the input waveform in the data record, and F_s is the sampling

frequency. Additionally, both the signal generator and the clock source used to trigger the sampling of the ADC should be phase-locked with a ultra-stable reference signal. These two conditions ensure coherent sampling that provides the best results to accurately measure the noise and distortion spectral components in the FFT. In these tests we satisfy the second condition using the reference signal provided by the Hydrogen Maser. But equation (1) is not completely respected since the frequency increments of the signal generator don't allow to reach the required precision.
Coherent sampling cannot be achieved, hence a window weighting function (see Paragraph 5.1) is applied to the time record to minimize spectral leakage. Windowing consists of multiplying the data in the time domain by a suitable window function with low-side lobes in order to resolve the noise and harmonic components in the frequency spectrum. Further information and details on how to choose the right FFT window function can be found in (Harris, January 1978).
While the signal generator is connected to an ADU board input, all the other inputs are terminated to 50 Ohm. Tests are repeated for all the ADU board inputs to evaluate the performances of each input chain and measure the cross-talk between them.
Except for IIP2 and IIP3 (two-tone analysis), the performances are measured in two frequency bands:

- 50-375 MHz ("Low frequency band") sampling data at 800 MSPS (1st Nyquist zone);
- 375-650 MHz ("High frequency band") under-sampling data at 700 MSPS (2nd Nyquist zone)

with segmented frequency sweeps setting a step size of about 1 MHz. The second and third-order input intercept points are computed on just one point of the low band and one point of the high band. The adopted frequencies of the two tones (equalized at the exactly same level after filter attenuation) are: 184 and 187 MHz for low frequency band, and, 500 and 503 MHz for high frequency band, always following equation (1) for frequency calculation, as said before.

3.2 Hardware test set-up

The basic setup (Figure 7) for dynamic testing includes a signal generator, band-pass filter, power meter (or spectrum analyzer), low noise power supplies, stable reference signal, ADU Board under test and PC/workstation for instrument control, data acquisition and data analysis.
Single-tone tests are performed as summarized here below (details will be given in next sections):

- A PC/workstation controls the signal generator and the power meter (or spectrum analyzer) via GPIB.
- For every frequency spanning the bandwidth, the PC/workstation sets a frequency and a nominal amplitude of the signal generator and then corrects iteratively the amplitude itself by reading the level with a power meter (spectrum analyzer). This loop process ends when the ADC input receives a signal with a level of about -1 dBFS within ± 0.08 dB of error. So the input signal amplitude is constant across all frequency range.
- ADU board FPGA stores time domain data in a 2MByte BRAM and sends UDP packets through 1Gbit Ethernet link.
- The PC/workstation gets UDP packets, checks for data integrity and saves files.
- Software routines (Matlab) process data and compute some parameters to evaluate the performance over the bandwidth (SNR, SFDR, SINAD, ENOB, etc…).

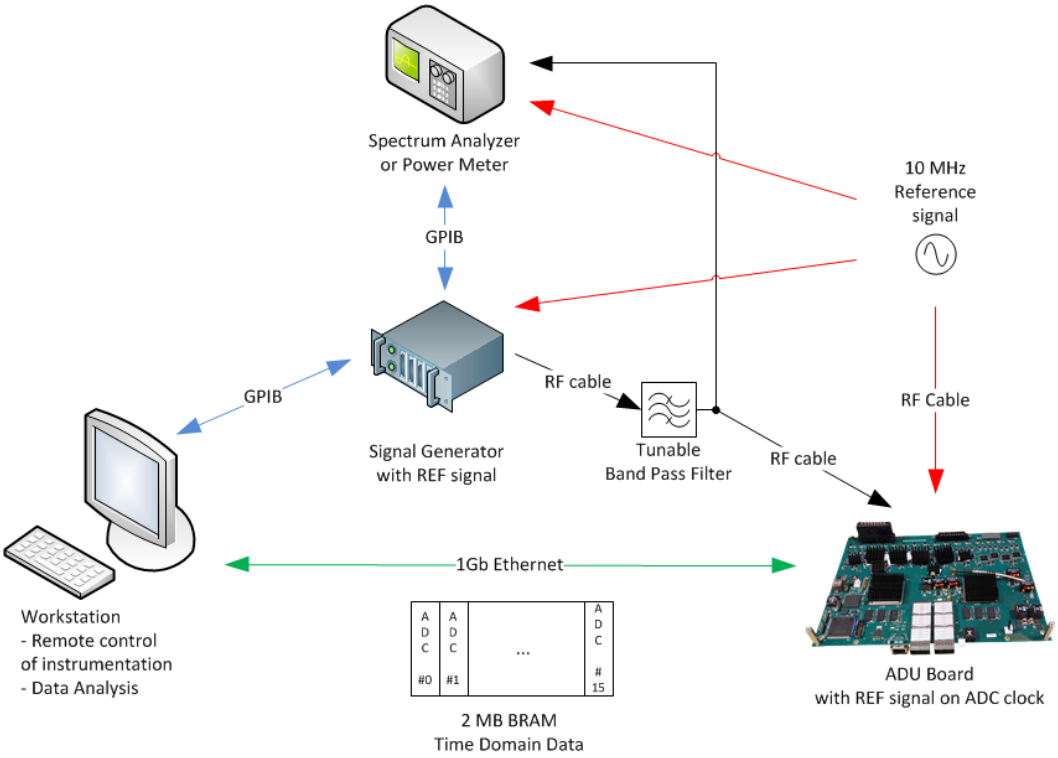


Figure 7: Block diagram of hardware test set-up.

As stated in Paragraph 1.2, the test session we are describing in this document has the goal of measuring the performances of the board including the harmonics and spurious signals generated by the device under test itself. Therefore we have to ensure that the signal source is as “clean” as possible, not generating this kind of undesired signals: for this reason it has to be properly filtered.
Also it is necessary to verify that the test environment is not affected by RFI that could invalidate the measurements. For this reason it is recommended to perform a preliminary RFI monitor campaign (as described in Appendix in Chapter 9).
Gain flatness measurement of the ADU board should not be subject to the filter response and the stability of the signal generator RF output level across the frequency range. So the system must be controlled in closed loop to guarantee a constant level of the signal at the ADC input, usually set to -1dBFS, both for single-tone and two-tone analysis (see Chapter 4.2).
The signal generator is locked to a very stable and precise frequency reference (10 MHz) provided by the Hydrogen Maser. This is important in order to have a high level of spectral purity and to reduce the phase noise. The same reference signal is used to lock the PLL that generates the ADC clock of the ADU board, improving the precision of ADC sampling. Without this precaution the spectrum would be affected by phase noise and spurious signals then corrupting the measurements.
In the case a spectrum analyzer is present in the chain, the reference signal should be connected to it as well.
The test bench prepared for ADU board measurements is visible in Figure 8.

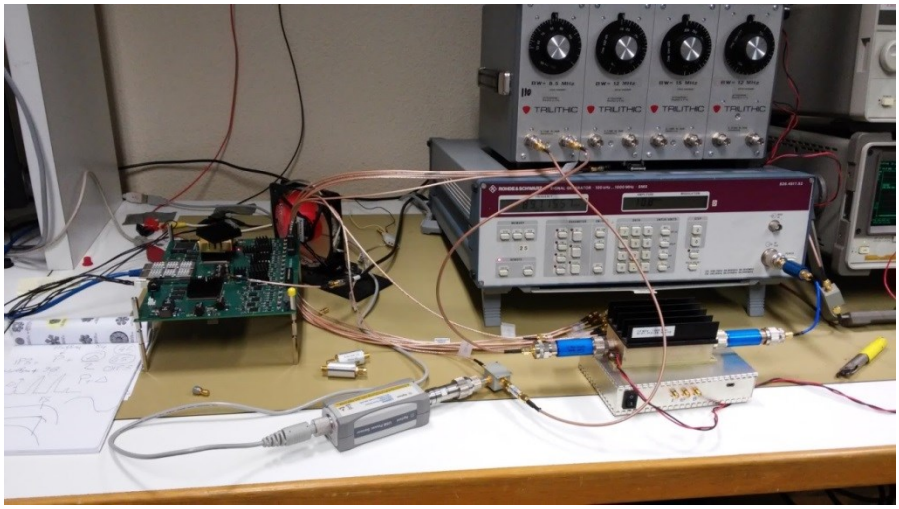


Figure 8: Test bench for ADU board measurements

3.2.1 Signal generator

All the instruments used to measure the ADU performance have been individually tested before choosing the best setup. First of all we have compared all the signal generators and clock synthesizers of our lab taking into account the most important parameters such as phase noise, harmonics and sub-harmonics spurious signals and also the maximum output power and the frequency and power level step size.
One fundamental requirement is the programmability of the device to set up a system as more automated as possible.
The choice was for the Rohde&Schwarz SMX Signal Generator (Figure 9).

Figure 9: Rohde&Schwarz SMX signal generator.

The main characteristics are shown in the next table (Table 2).

Frequency Range	100KHz-1GHz
Harmonics	<-30 dBc (for level <10 dBm)
Nonharmonics At >5 KHz from carrier	F < 31.25 MHz < -60 dBc F < 125 MHz < -72 dBc F < 250 MHz < -72 dBc
SSB phase noise carrier offset 20 KHz, 1 Hz BW guaranteed	F < 31.25 MHz < -130 dBc F < 125 MHz < -130 dBc F < 250 MHz < -138 dBc
Broadband noise (carrier offset > 2 MHz, 1Hz BW)	F < 31.25 MHz < -145 dBc typical
Residual FM, rms	0.3 to 3 KHz(CCITT): F<250 MHz <2Hz 0.03 to 20 KHz: F < 250 MHz < 5 Hz
VSWR	< 1.5 (level <= 0dBm), < 1.8 (level > 0 dBm)

Table 2: Main characteristics of Rohde&Schwarz SMX signal generator.

3.2.2 Filters

Harmonic performance of generators is typically not as good as the intrinsic linearity of a given ADC, making the use of filters between the signal generator and the analog input of the ADU board essential for precise measurements.
The Trilithic tunable narrow band-pass filter was used for device testing (Figure 10).

Figure 10: Trilithic tunable band-pass filter.

This filter can operate in four banks with slightly different passband bandwidths, as reported in the Table 3.

Band #	Lower bound (MHz)	Upper bound (MHz)	Bandwidth (MHz)
1	55	110	8.5
2	110	220	12
3	220	440	15
4	440	900	12

Table 3: Bandwidth characteristics of Trilithic filter banks.

The filter response presents ripples across bandwidth and may change a lot depending on the position of the tune. Following pictures show examples of the filter response at different tuned central frequencies. As you can notice in some cases the filter $|S_{21}|$ at central frequency is more attenuated than at the rest of the band.

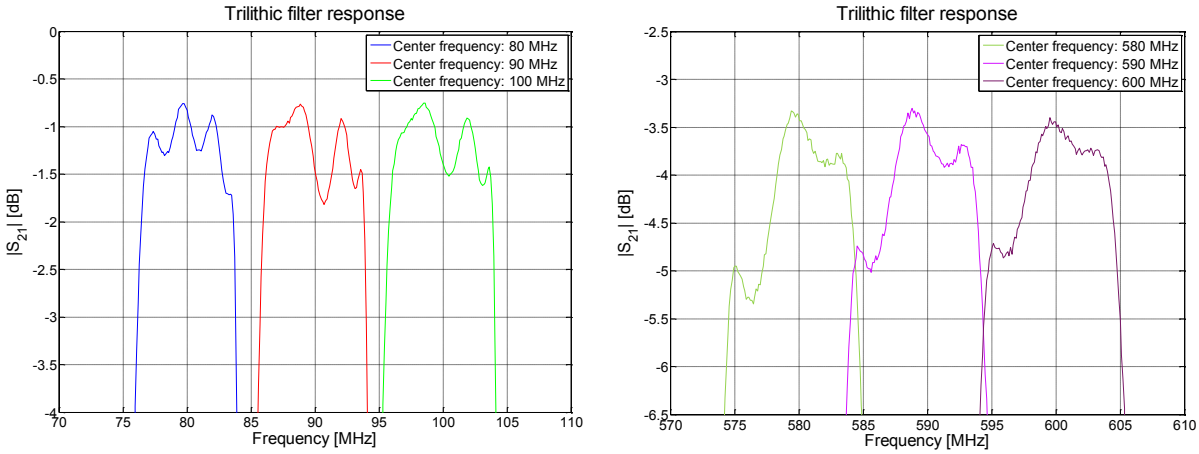


Figure 11: Insertion loss of Trilithic tunable band-pass filter at different tuned central frequencies.

This great variability of the filter response has to be compensated by a closed loop controller (see Paragraph 4.2) that continuously measures the signal level after filters and adjusts the output power of signal generator in order to maintain a constant signal level at the ADU board input.
Since the Trilithic tunable band-pass filter has performance degradation around the 4th harmonic and in some cases also sub-harmonic, a set of high-pass filters and low-pass filters were added to obtain the level of spectral purity required by the application across all the test frequencies.
The following table shows the high/low-pass filters used over the frequency range:

Band #	Start Freq. (MHz)	Stop Freq. (MHz)	High Pass Filter (Mini Circuit)	Low Pass Filter (Mini Circuit)	Bandwidth (MHz)
1	55	110		SLP-100	<108
2	110	220	SHP-100	SLP-250	82-250
3	220	440	SHP-200	SLP-450	164-440
4	440	550	SHP-200	SLP-550	164-570
5	550	650	SHP-500	SLP-1000	454-990

Table 4: High/low-pass filters and the relative working band.

Filters are the only components of the chain without a remote control and require considerably manual operations during measurements, making them very time-consuming.

3.2.3 LNA

Tests on no-ADA version of ADU board need an external low noise amplifier that permits the signal generator output level to reach the -1dBFS ADC level. This amplifier must necessarily be added between the signal generator and the filter stage in order to strongly attenuate potential spurious signals.
Minicircuits ZHL-2-8-N has been chosen for this purpose because it is a low noise amplifier with +6dB of noise figure and an high gain of +29dB, working between 10 and 1000MHz. It has also high performance in terms of non-linearities.

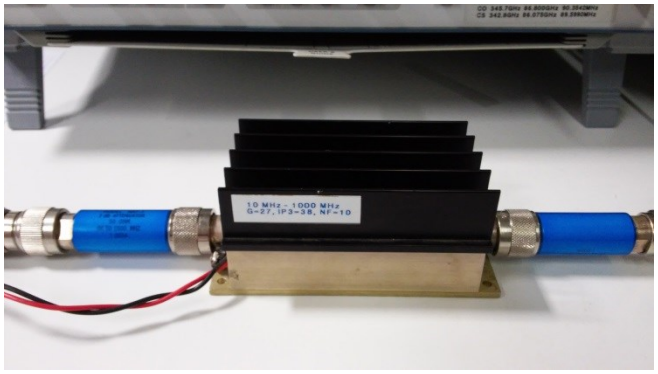


Figure 12: Low Noise Amplifier.

3.2.4 Power meter

The selected power sensor is Agilent U2004A that works from 9kHz to 6GHz, with a power range between -60dBm and +20dBm. It has the capability of internal zeroing and can be connected to a computer through USB port.

4 Control software

4.1 Firmware

The ADU board configuration registers and the device control signals are managed by the CPLD. This device has an internal flash and is auto-configuring at the board start-up. It provides Ethernet user interface and bus lines to connect all the devices configuration interfaces.
In particular the CPLD main tasks are:

- the remote board control, UDP command interface;
- FPGA management bus for USER FPGA register access and debug purpose;
- FPGA fast configuration, reconfiguration and monitoring;
- monitor of temperatures, voltages and currents via I2C bus;
- I2C bus connected with QSFP+;
- SPI buses for board non-volatile configuration data storage, configuration of analog amplifiers, ADCs (see Appendix in Chapter 8) and acquisition PLL.

The management user interface is based upon the Ethernet-UDP IP core, which allows executing sequences of memory mapped bus accesses from a remote console.

The Xilinx UltraScale FPGAs are two identical devices that provide suitable and efficient resources to implement the main board data processing. The two FPGAs have a compatible pinout and can share the same configuration firmware. In fact each of the two FPGAs can manage sixteen data links to receive data from the ADCs and provide the required elaboration.
FPGA firmware for ADU board 1.0 was developed as a very preliminary and limited version without many IP cores (e.g. to address external DDR memories, interface with high speed QSFP+ links, ecc…).
The planned tests require both time domain and frequency domain analysis on data sampled by ADCs. For implementation convenience, these analysis algorithms have been developed in a computer rather than with a dedicated FPGA firmware. So the FPGAs are used only to acquire ADC samples (via JESD204b lanes), to buffer into 2MB Block RAM logic and to send the time domain data in UDP packets through the 1Gbit Ethernet interface. Once the buffer is completely filled the memory is accessed for reading and data are sent in multiple UDP packets tagged with a very short header (sequence counters and flags). The firmware is quite flexible, allowing to select how many (from 1 to 16) and which ADC input streams are written into 2MB internal memory.

4.2 Instruments management

As previously mentioned, the power level of the signal injected into ADU board must be equal to a constant value of -1 dBFS for every frequency spanning the bandwidth of test. There are some factors that affect this level making it non-constant like the non-stability of the signal generator RF output and the insertion loss of the filters that is variable in frequency (as said before).
Thus a control procedure that measures the level of the signal and corrects it to a constant target value is needed. This measurement is performed by the USB power sensor connected to a directional coupler (Minicircuits ZEDC-15-2B).

Figure 13: USB power sensor (Agilent U2004A) connected to a directional coupler for the measurement of the signal power level.

This power sensor can be easily controlled with python libraries (PyVisa) which instantiate a GPIB object over USB and provide the methods to change attributes (e.g. the timeout of instrument response) and to read the power level (dBm).

```
1 import visa
2 rm = visa.ResourceManager()
3 rm.list_resources()
4 pow = rm.open_resource(u'USB0::0x0957::0x2D18::MY53040009::INSTR')
5 pow.timeout=90000
6 print("\nPower %3.2f dBm\n"%(float(pow.query('MEASURE?'))))
```

```
D:\SKA-TPM\PythonScript\sdp>python read_power.py
Power -12.46 dBm
```

Figure 14: Screenshots showing some commands to control a power meter with Python scripting.

When using a directional coupler (like the one in Figure 15) it is necessary to take into account both the coupling loss and the insertion loss, i.e. $|S_{23}|$ and $|S_{13}|$ respectively.

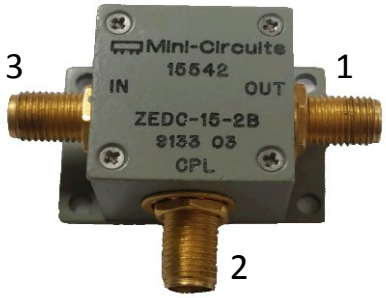


Figure 15: Directional coupler (Minicircuits ZEDC-15-2B).

The following figure shows the coupling loss and insertion loss (in frequency) of the directional coupler used for the measurements. Note that both curves are not flat even if the difference is quite small. Nevertheless it has to be considered during the correction procedure.

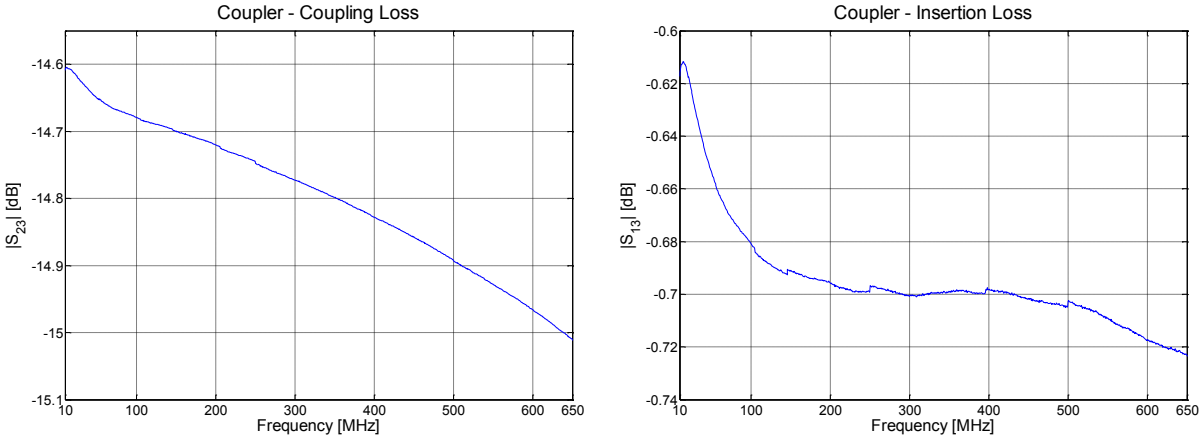


Figure 16: Coupling loss and insertion loss of the directional coupler.

Considering these relations:

$$S_{cpl} = S_{in} + CL \qquad (2)$$

$$S_{out} = S_{in} + IL \tag{3}$$

where S_{in}, S_{cpl} and S_{out} are respectively the input signal (port 3), the coupled signal (port 2) and the output signal (port 1) of the directional coupler (Figure 15).
It follows that:

$$S_{out} = S_{cpl} - CL + IL \tag{4}$$

where we can consider

$$Corr\_Factor = IL - CL \tag{5}$$

so (4) becomes:

$$S_{out} = S_{cpl} + Corr\_Factor \tag{6}$$

Note that (6) can also be expressed as:

$$P_{corr} = P_{read} + Corr\_Factor \tag{7}$$

where P_{corr} is the corrected power and P_{read} is the power read by the power sensor.
Coupling loss and insertion loss curves are measured by a Vector Analyzer (Agilent N5249A PNA-X) and stored in two files. Starting from these data the correction algorithm interpolates frequency-by-frequency the *Corr_Factor* level using linear fitting method (two-point form of a linear equation):

$$\frac{y - y_1}{y_2 - y_1} = \frac{x - x_1}{x_2 - x_1} \tag{8}$$

where (x_1, y_1) and (x_2, y_2) are two points on the line with $x_2 > x_1$.

The algorithm is very simple and it can be described with the following steps (see also the block diagram of Figure 17):

1. the frequency of the signal generator is set taking the value from a predetermined subset, the amplitude value is set to an arbitrary fixed level;
2. the power sensor measures the signal level at the coupled port of the directional coupler and this value is corrected with the correction factor (see equation (7)) that depends on frequency, as shown in the two previous plots;
3. if the difference between the value of the corrected measurement (P_{corr}) and the value of the target level (P_{target}, -1 dBFS) is not less than ±0.08 dBm then this difference is applied to the previous value of the signal generator. This operation is repeated until the condition is true; Since we are using a band pass filter, when the frequency of the signal generator is in the stop band of the filter the corresponding RF output power is very attenuated. Consequently, the correction algorithm fails because the maximum output power level of signal generator (+13 dBm) is not sufficient to compensate the attenuation of the filter. So it is necessary to manually tune the filter as long as the signal generator frequency is in the pass-band.

4. when the previous condition is satisfied, UDP packets containing time domain data for this frequency are acquired and saved into files. This operation is repeated 10 times in order to let FFT spectrum be averaged to reduce noise in the analysis phase.
5. points from 1 to 4 are repeated until the set of frequencies is finished.

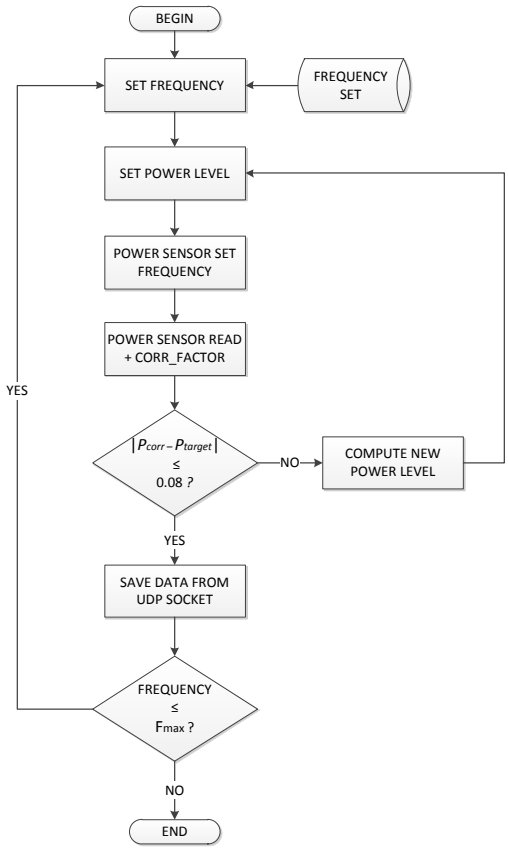


Figure 17: Block diagram describing the state machine of the test.

Figure 18 demonstrates the result obtained using this correction procedure: while the RF output of the signal generator (after correction) is not constant in frequency to compensate insertion loss of filters and the non-stability of the signal generator (blue line), the power level measured at the ADU board input is always constant (red line).

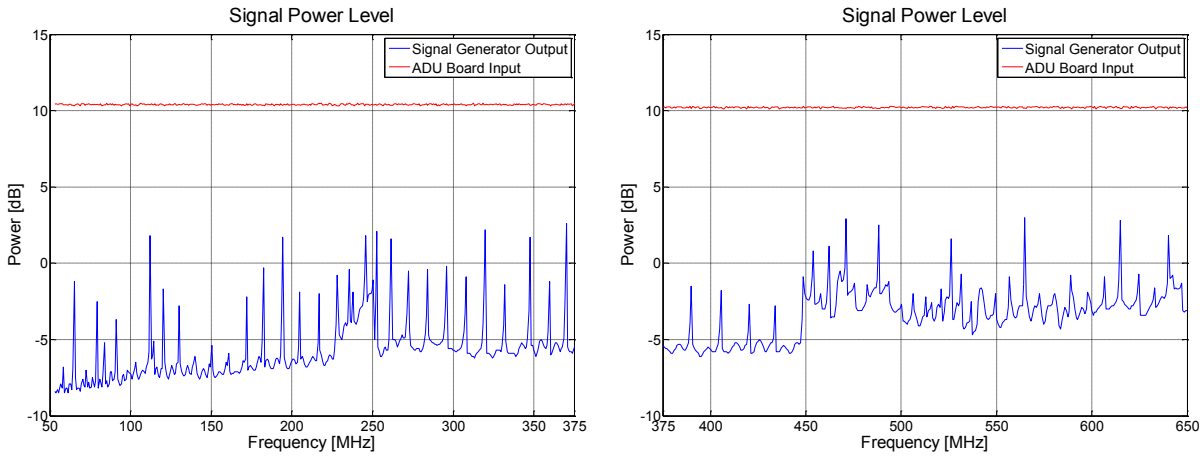


Figure 18: The blue line shows the signal generator corrected set-point in order to achieve the constant -1 dBFS level for the ADC input. The red line is the corresponding (constant) power level at the ADU board input.

5 ADU Board performance evaluation

5.1 Data analysis software

Some software routines (MATLAB®) were specifically developed in order to calculate the performance parameters described in the previous paragraph (section 3.1). After data collection campaign is completed for every analog input and for every frequency of the bandwidth, this software can be executed. The main steps are summarized in Figure 19.

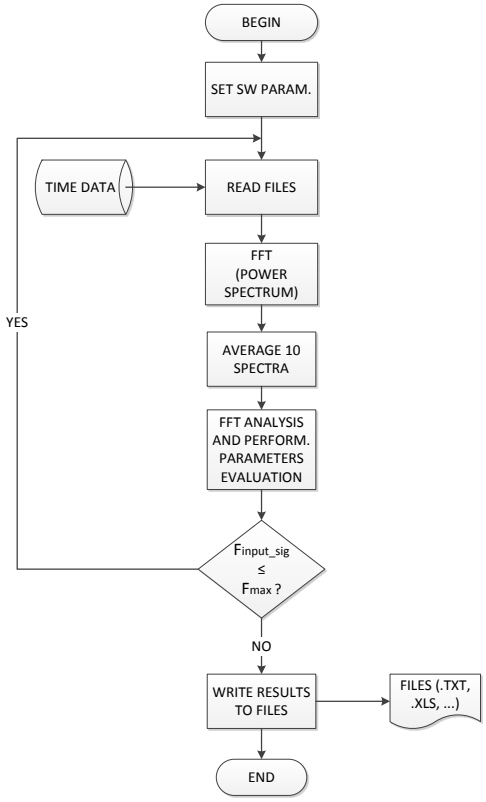


Figure 19: Flowchart of data analysis software

First of all some software parameters, listed in Table 5, have to be set. If we want to test the board in the frequency range 50-375 MHz, we have to assign Fs = 800 MSPS and Nyquist Zone = 1, whereas if the frequency range of interest is 375-650 MHz we have to choose the combination Fs = 700 MSPS and Nyquist Zone = 2.

SW Parameters	
F_S	Sampling Frequency (default 800 MSPS)
Nyquist Zone	1 for sampling in the first Nyquist Zone 2 for sampling in the second Nyquist Zone
N. Inputs	Number of inputs that are acquired (default 16)
Input Signal	What input is feeded with signal generator
Dir	Path where files can be read
N. Input Tones	1 for single-tone FFT analysis 2 for two-tone FFT analysis
HD Order	Number of Harmonic Distortion Products to be considered (default 6)

Table 5: List of software parameters that need to be set up at the beginning of software execution.

Also the number of analogue inputs whose data have been simultaneously acquired has to be specified. This parameter is closely related to the frequency resolution of the FFT since data acquisition buffer is limited to 2 Mbyte (see paragraph 4.1). In particular we have the possibilities listed in Table 6.

N. Analogue Inputs	N. points of FFT	Frequency Resolution	
		BW=50÷375 MHz	BW=375÷650 MHz
16	131072	6.104 KHz	5.341 KHz
8	262144	3.052 KHz	2.670 KHz
4	524288	1.526 KHz	1.335 KHz
2	1048576	762.94 Hz	667.6 Hz
1	2097152	381.5 Hz	333.8 Hz

Table 6: FFT frequency resolution for all the possible cases.

Moreover it is necessary to indicate what analogue input is connected to the signal generator respecting the numbering 0÷15. Finally you have to set also the directory where the input files are stored, if only one tone is injected into the board (single-tone FFT analysis) or if there are 2 (two-tone FFT analysis) and the number of Harmonic Distortion products that have to be considered in the Fourier analysis.
Starting from the first analogue input under test and from the first frequency of the range, data files are read and copied into local memory. Then a real Fast Fourier Transform with a Blackman-Harris window is applied to time domain data. Once all the power spectra (10) have been calculated, they are averaged.
In a debug version of the software there is the possibility to plot all the spectra in order to check the level of the input signal and verify if all the hardware test setup is working properly.
The averaged power spectrum is the basis for calculating all the performance parameters described in section 3.1.
The sequence of operations from reading data onwards is repeated for all the frequency set of the two bandwidths:

- 430 frequencies for the 50-375 MHz bandwidth;
- 370 frequencies for the 375-650 MHz bandwidth.

Finally all the results are written in a output file (.xls by default or you can choose another format).
The procedure above described provides the characterization of only one ADU Board input, so you have to repeat all these steps for all inputs to fully test the board.

Several functions that implement the algorithms for the calculus of parameters have been developed, tested and validated for this particular scope. Debug and validation phases were accelerated with the use of Analog Devices evaluation board (Figure 20).
In fact, thanks to a commercial contract, Analog Devices provided us a high speed ADC FIFO evaluation kit (www.analog.com/FIFO) that includes a FPGA-based buffer memory board to capture blocks of digital data from high speed ADC evaluation board through FMC connectors, VisualAnalog® and SPIController software.
Basically the debug process was conducted in the following way: the evaluation board acquired some raw data, we processed it with the developed software routines and the results were compared with the ones obtained running VisualAnalog application. These operations allowed us to find and solve some bugs and consequently validate the data analysis software.

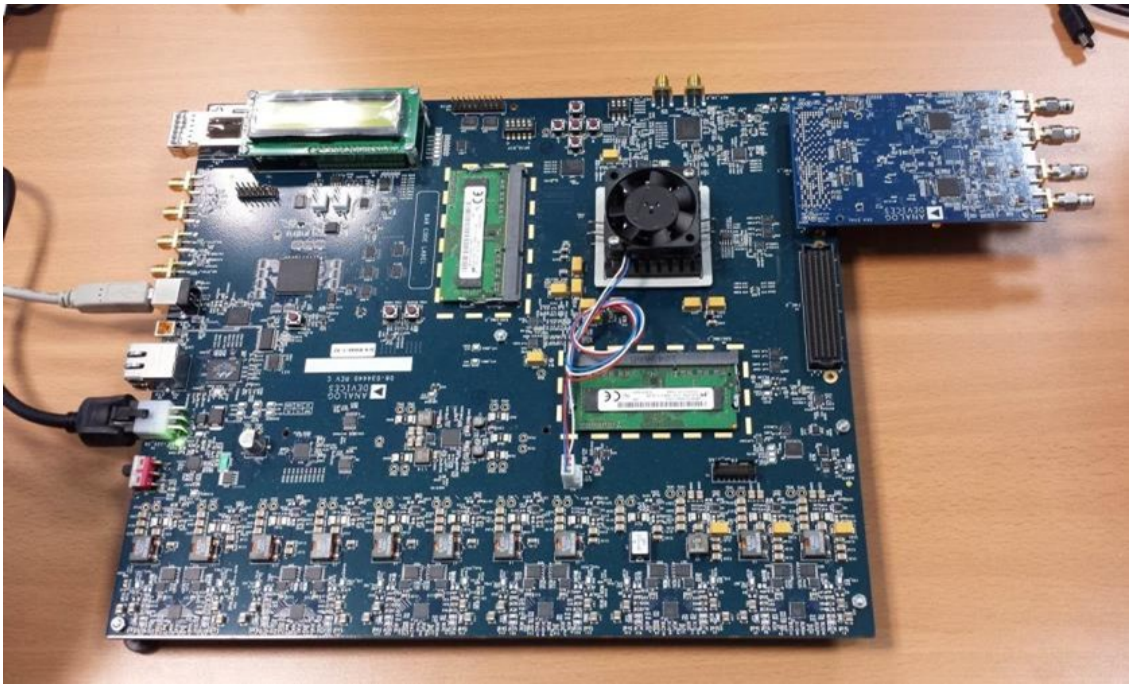


Figure 20: Analog Devices Evaluation Board.

5.2 Summary of performances

In this paragraph there is a collection of the principal evaluation parameters plotted in frequency for both the two ADU boards. The first part is relative to the low frequency band, the second one is dedicated to the high frequency band.

5.2.1 Low Frequency Band (50-375 MHz)

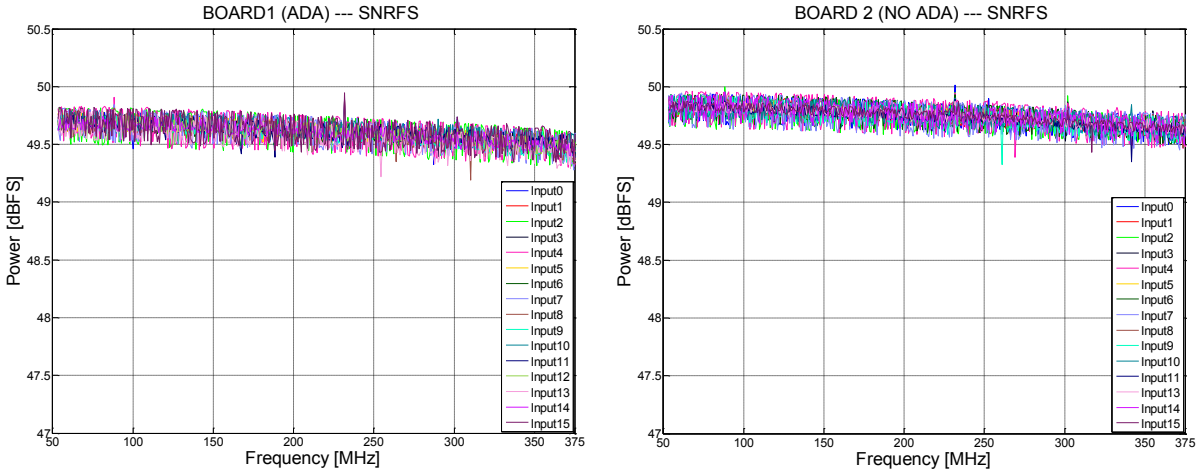


Figure 21: Signal to Noise Ratio referenced to Full Scale (SNRFS) in Low Frequency Band.

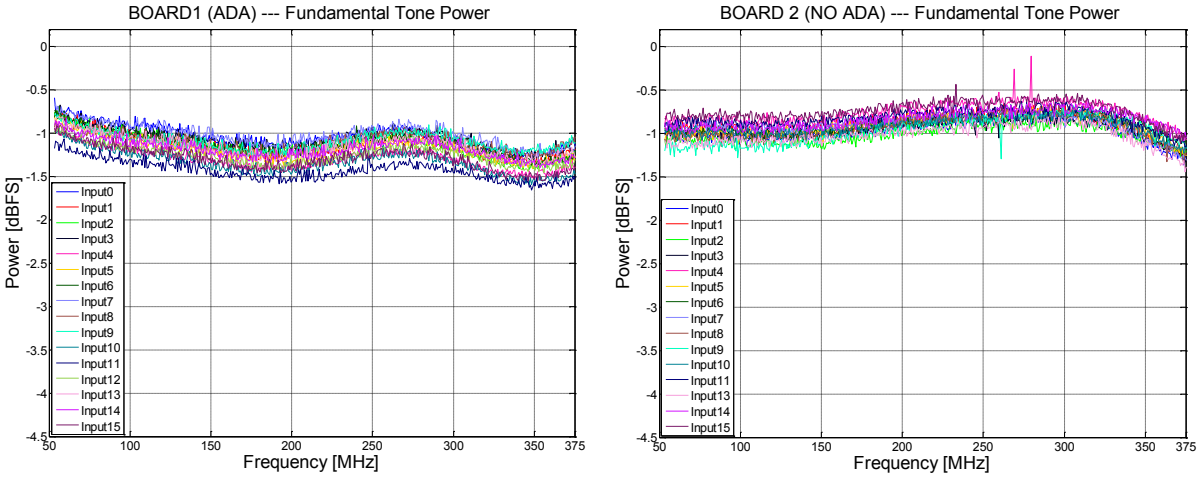


Figure 22: Gain Flatness in Low Frequency Band.

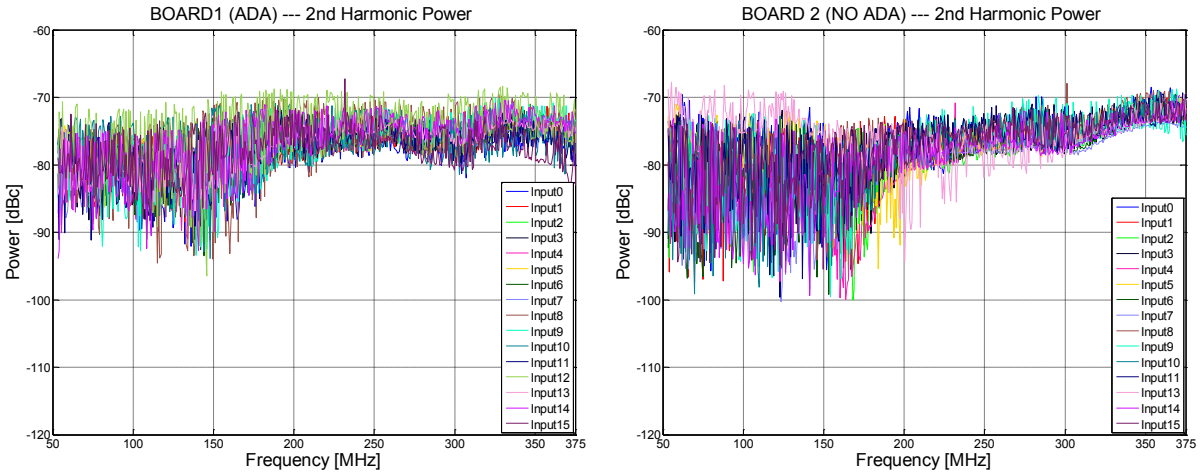


Figure 23: 2nd-order Harmonic Distortion Power in Low Frequency Band.

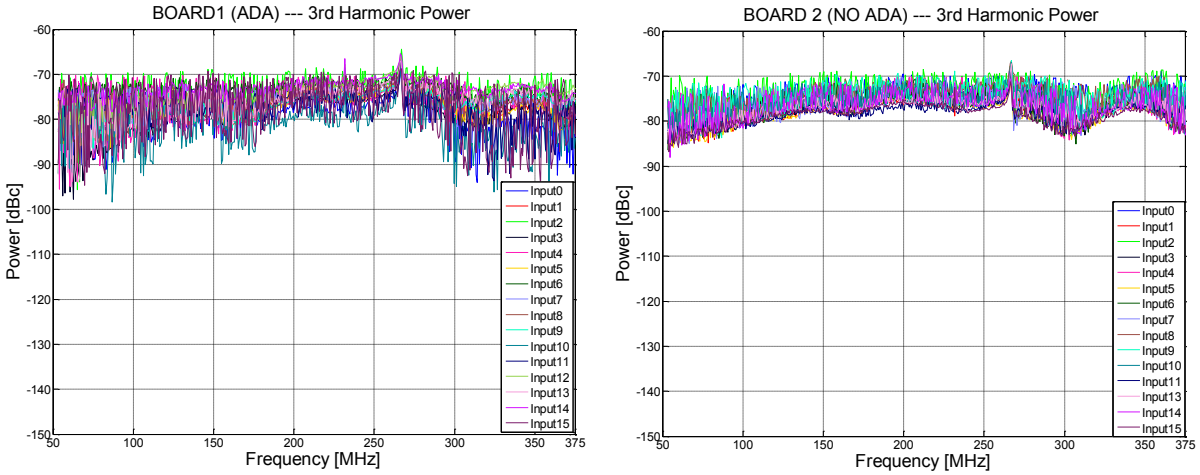


Figure 24: 3rd-order Harmonic Distortion Power in Low Frequency Band.

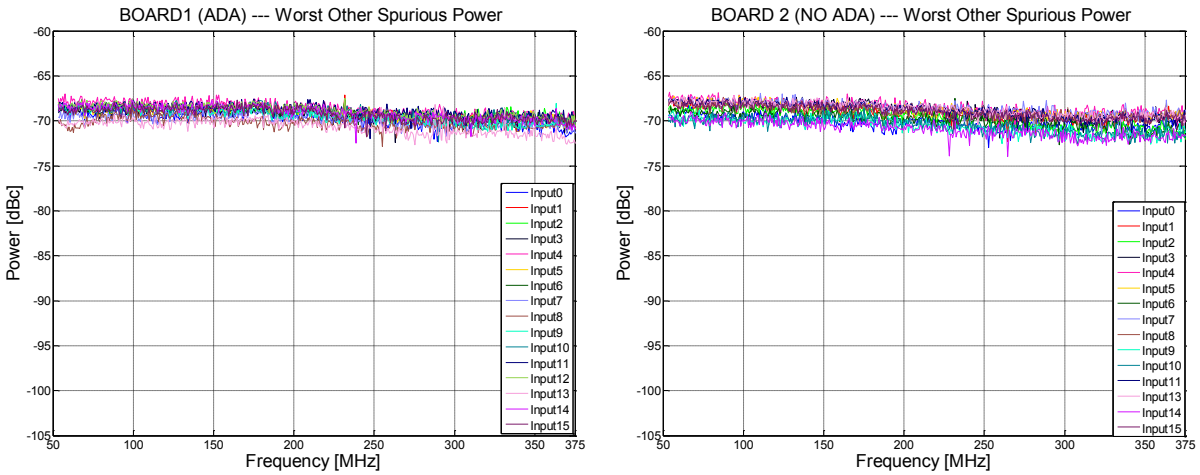


Figure 25: Worst Other Spurious Power in Low Frequency Band.

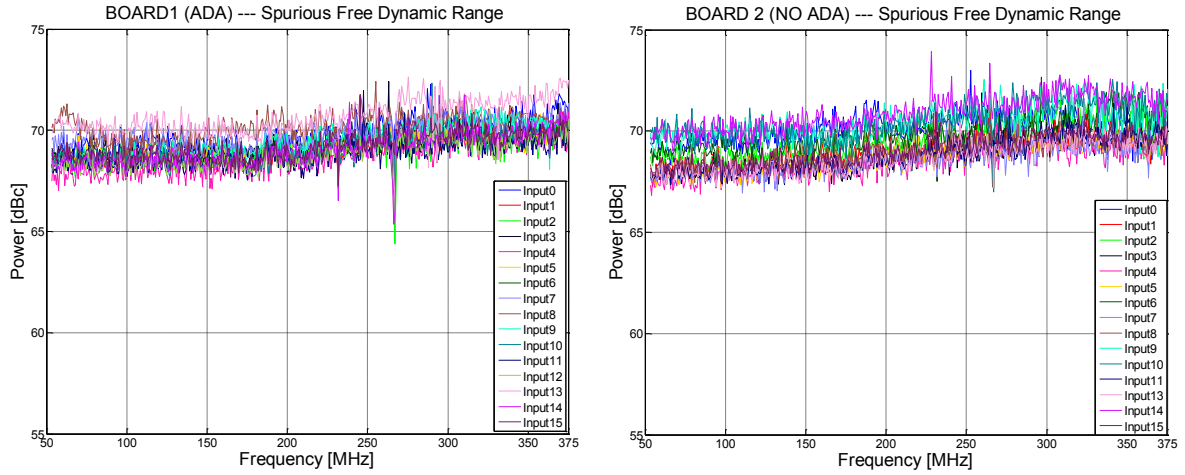


Figure 26: Spurious Free Dynamic Range in Low Frequency Band.

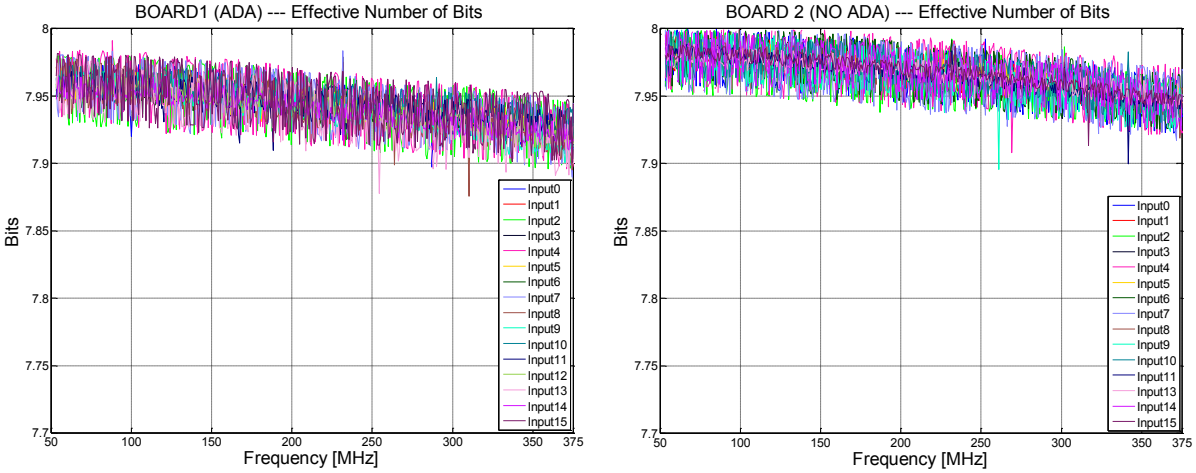
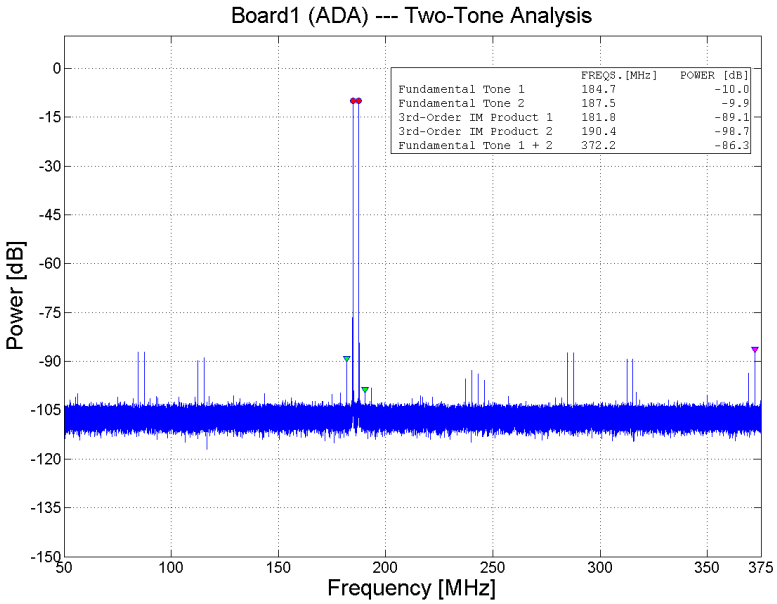


Figure 27: Effective Number of Bits in Low Frequency Band.



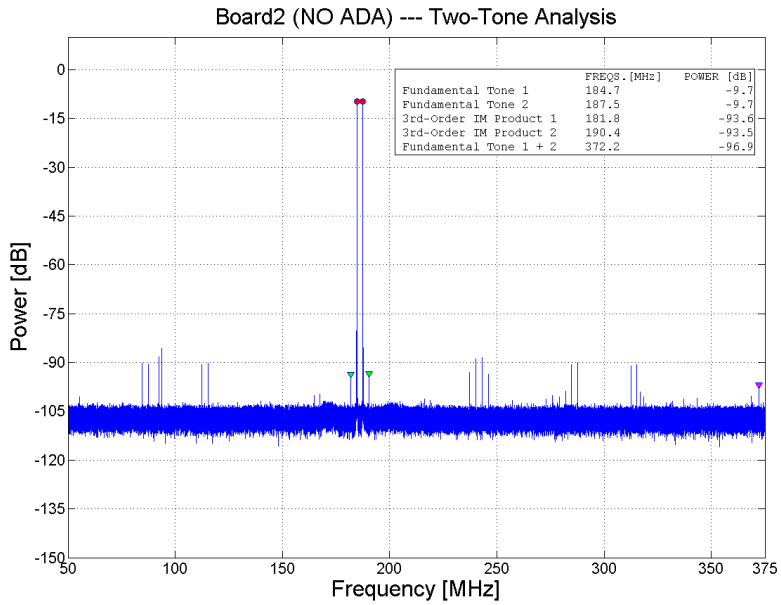


Figure 28: Power Spectrum with two tones injected in input for IP2 and IP3 measurement in Low Frequency Band.

5.2.1.1 Cross-Talk analysis in Low Frequency Band

Cross-Talk analysis is important to determine the interference (or mutual coupling due to electromagnetic interaction) between adjacent traces on the board. For this kind of characterization we drove the ADU board with the signal generator connected to one input and we measured the power level, relative to the frequency bin of the injected signal, from the other inputs.
Consider the numbering of the ADU board inputs as indicated in Figure 29, where the green boxes are the baluns, placed alternatively on top and bottom.

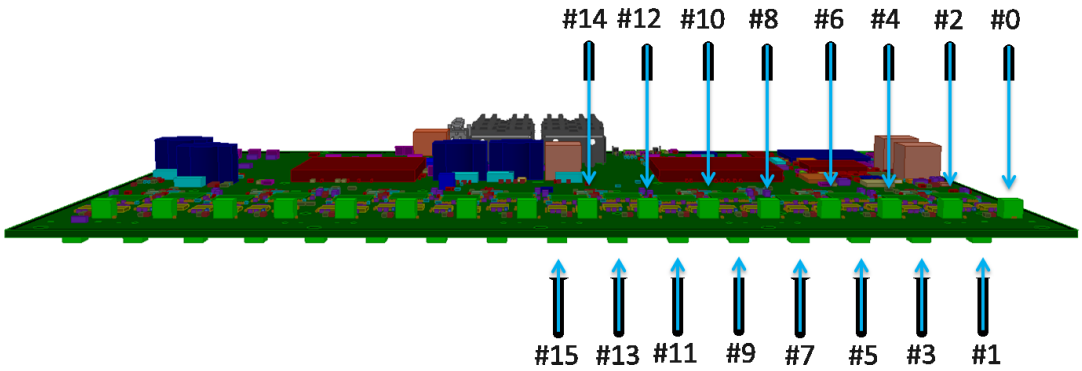


Figure 29: Numbering of the ADU board inputs adopted for Cross-Talk analysis.

The PCB traces that result more subject to Cross-Talk effects are the ones relative to inputs on top of the board (even numbers) and on the right hand side (the first 4 and in particular the n. #4 and #2). Next figure (Figure 30) gives an idea of the strongest interactions.

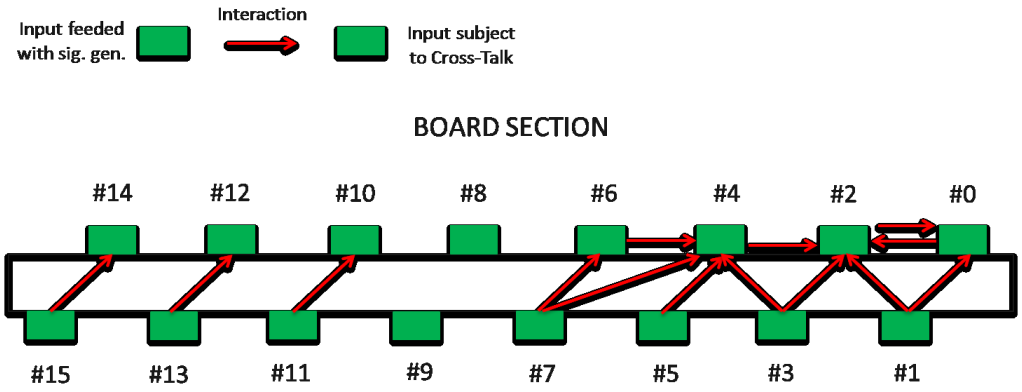


Figure 30: The strongest interactions between the traces of the board due to Cross-Talk effect.

In Figure 31 it is reported the worst case of this scenario for the two ADU boards: i.e. Cross-Talk "seen" by input #4 when the signal generator drives the other inputs. For both Board1 and Board2 the highest values are due to inputs #3, #5 and #6. This is very likely caused by the proximity of that traces in the PCB layout.

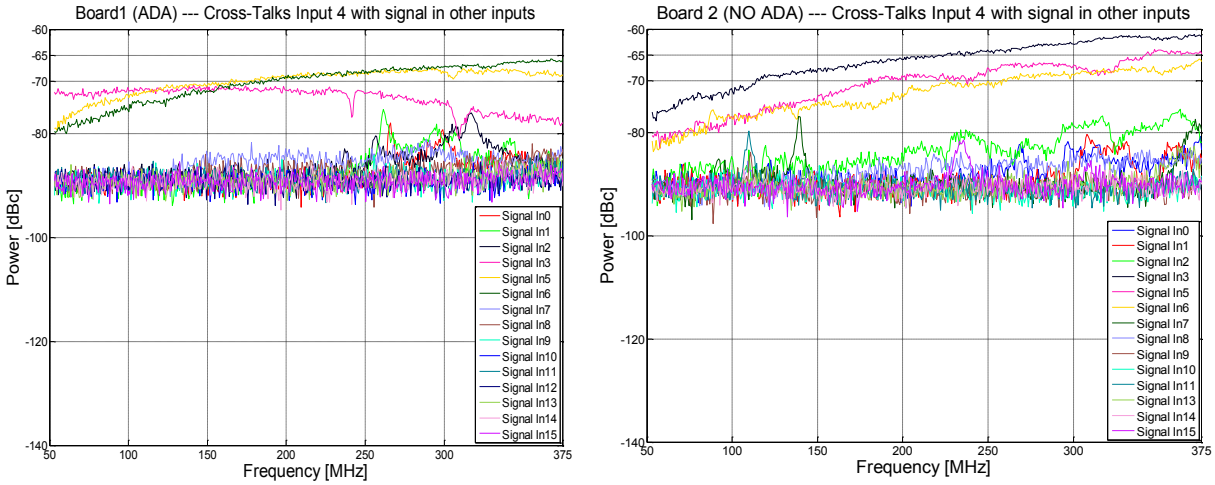


Figure 31: Worst case of Cross-Talk level in Low Frequency Band.

5.2.2 High Frequency Band (375-650 MHz)

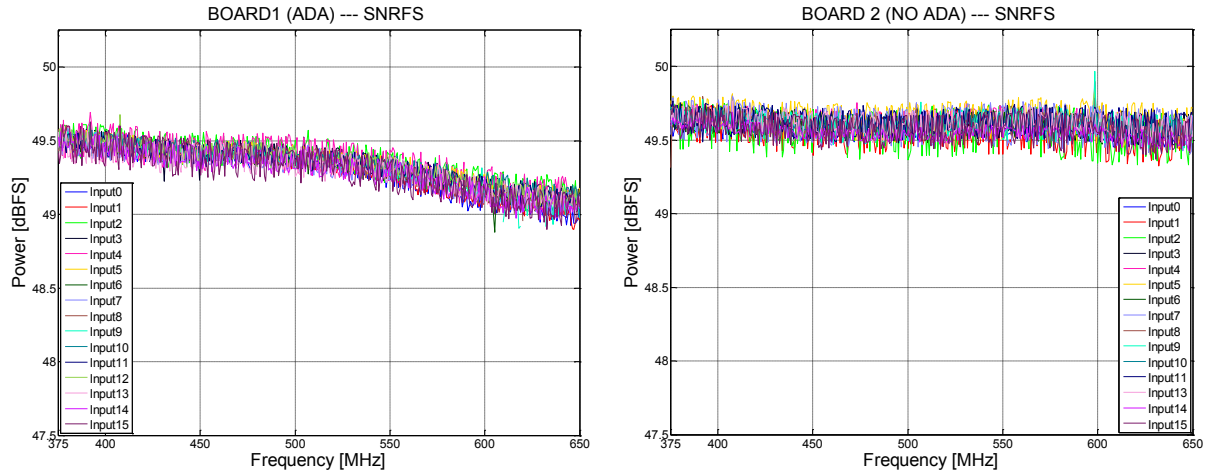


Figure 32: Signal to Noise Ratio referenced to Full Scale (SNRFS) in High Frequency Band.

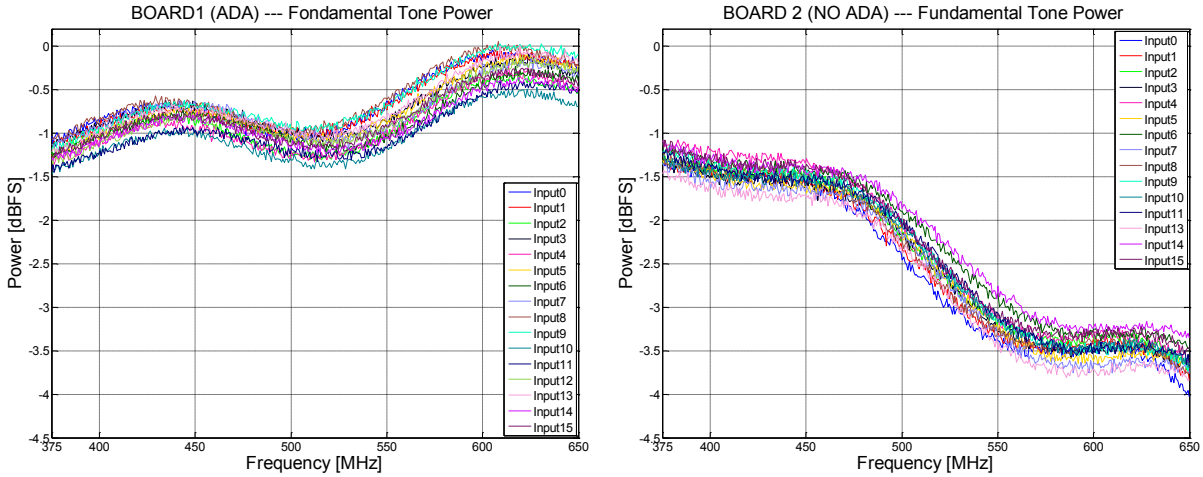


Figure 33: Gain Flatness in High Frequency Band.

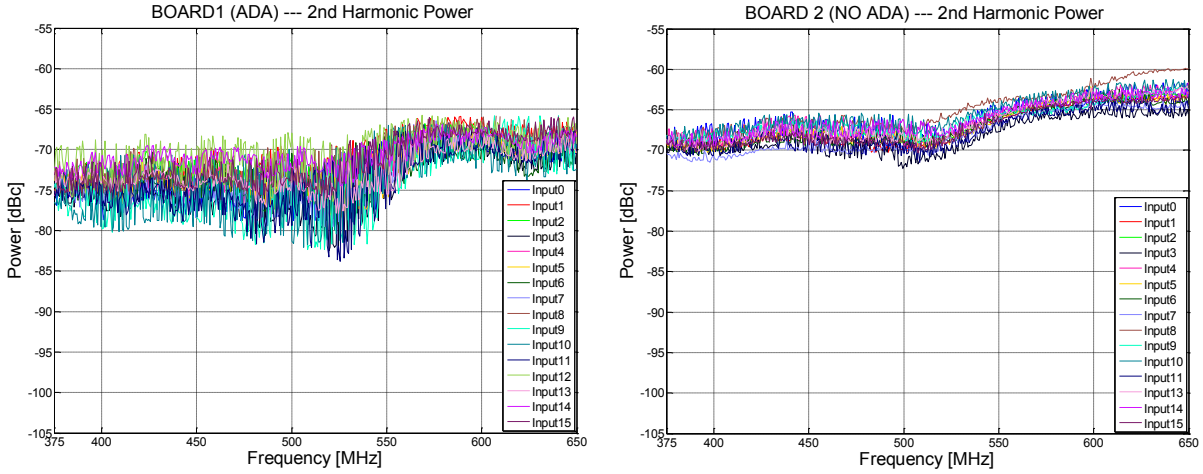


Figure 34: 2nd-order Harmonic Distortion Power in High Frequency Band.

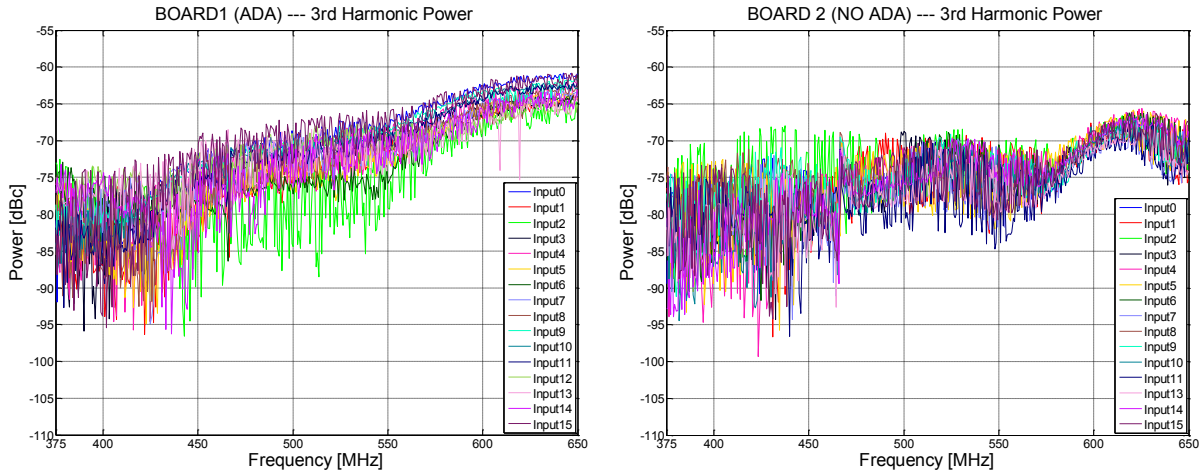


Figure 35: 3rd-order Harmonic Distortion Power in High Frequency Band.

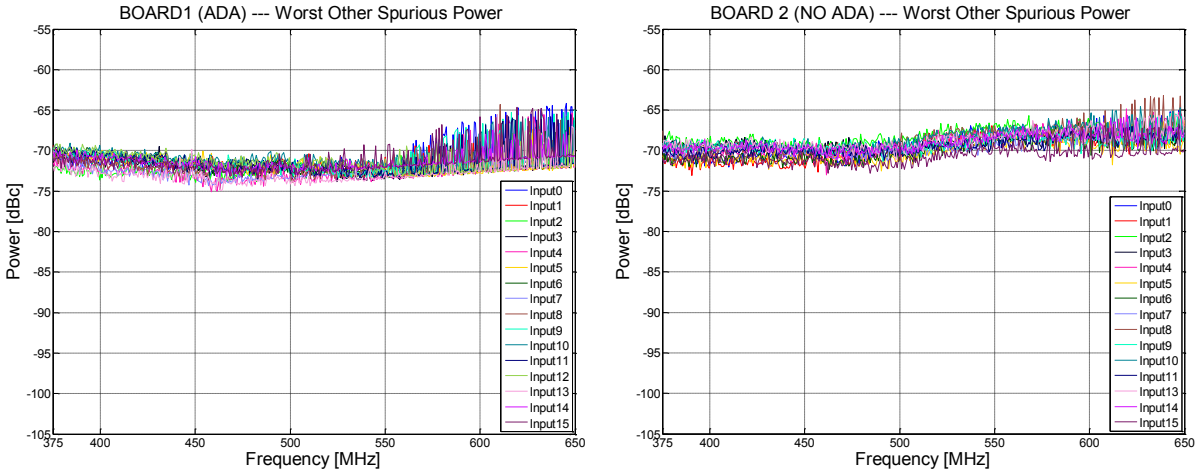


Figure 36: Worst Other Spurious Power in High Frequency Band.

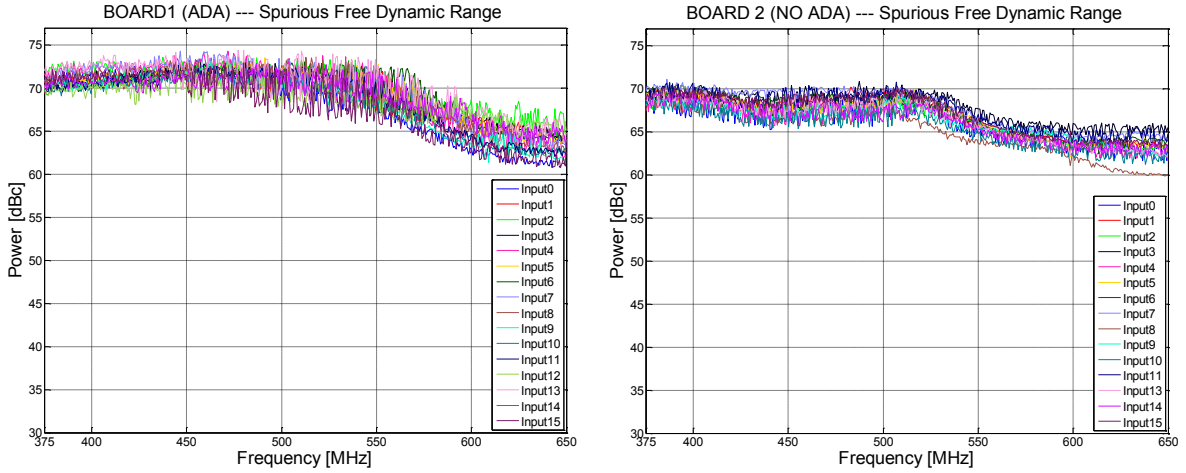


Figure 37: Spurious Free Dynamic Range in High Frequency Band.

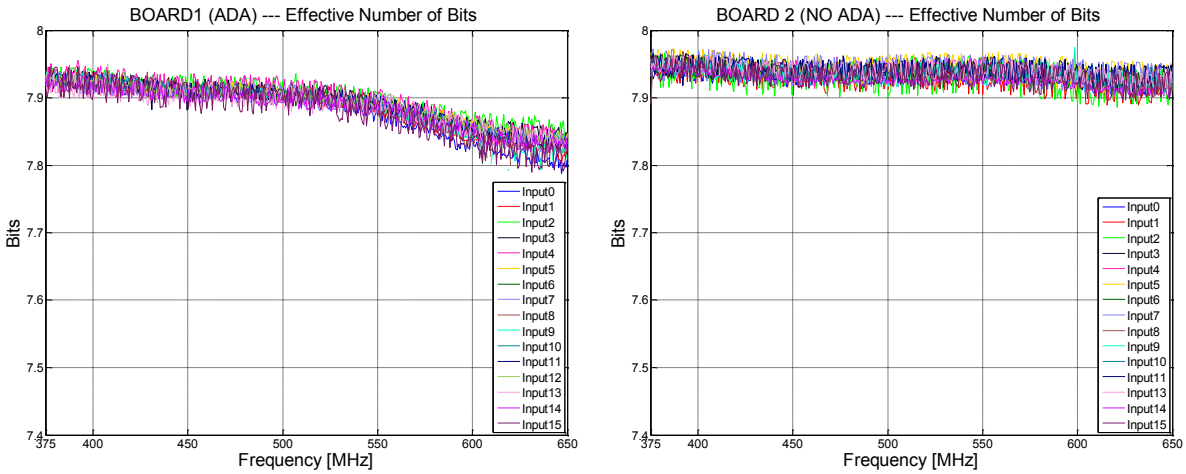


Figure 38: Effective Number of Bits in High Frequency Band.

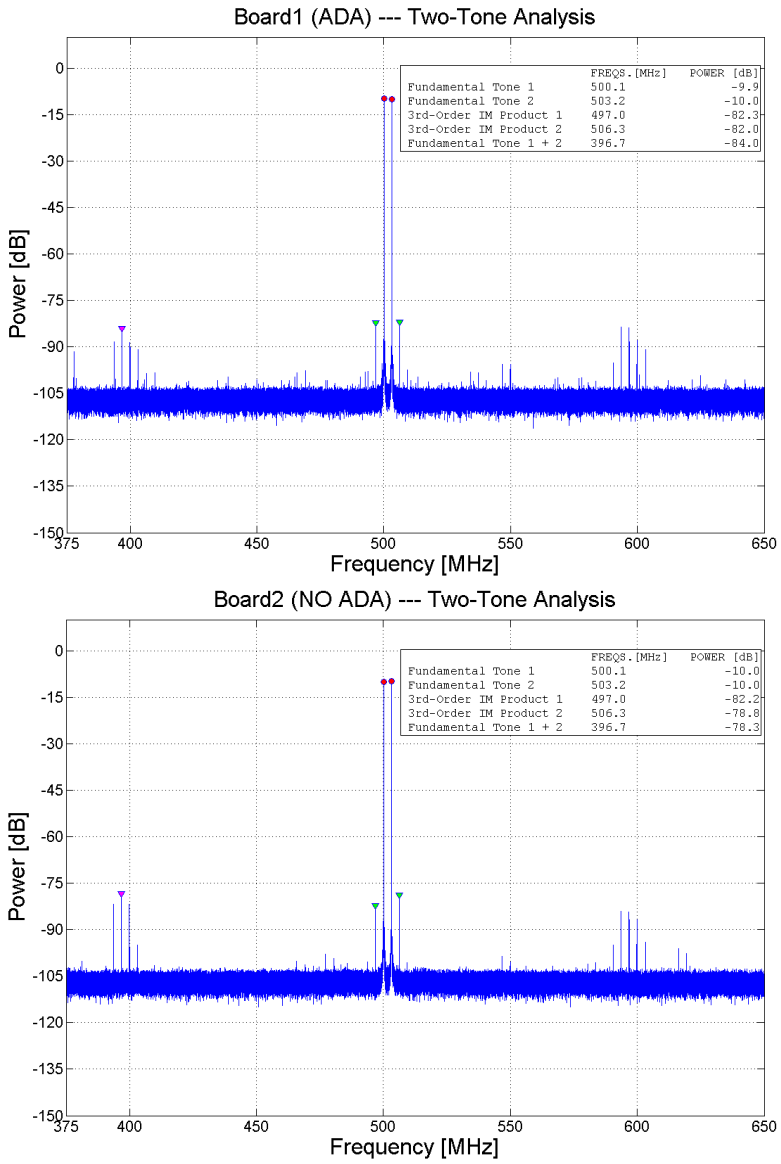


Figure 39: Power Spectrum with two tones injected in input for IP2 and IP3 measurement in High Frequency Band.

5.2.2.1 Cross-Talk analysis in High Frequency Band

The same considerations made for Low Frequency Band (paragraph 5.2.1.1) apply also for High Frequency band. In this case we can see from Figure 40 that for Board1 the highest Cross-Talk values are “felt” by input #4 due to the interaction with inputs #3, #5 and #6; on the contrary for Board2 the highest Cross-Talk values are “felt” by input #2 due to the interaction with inputs #1, #3 and #4.

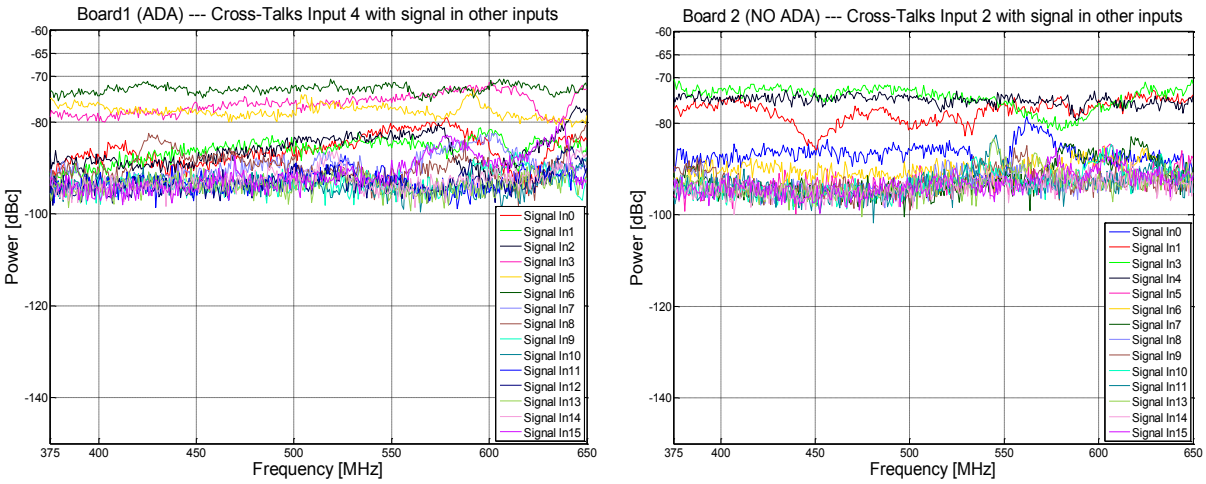


Figure 40: Worst case of Cross-Talk level in High Frequency Band.

6 Conclusions

Table 7 summarizes all the results obtained with the measurements performed on the two ADU boards and over the two frequency bands.

Fs: 800 MSPS --- BW: 50 ÷ 375 MHz		
ADC Performance Parameters	**ADU Board#1 (with ADA)**	**ADU Board#2 (without ADA)**
Signal to Noise Ratio referenced to Full Scale [dBFS]	≥ 49.19	**≥ 49.33**
Gain Flatness [dBFS]	≤ ±0.3573	**≤ ±0.343**
2nd-order Harmonic Distortion [dBc]	≤ -67.24	**≤ -67.74**
3rd-order Harmonic Distortion [dBc]	≤ -66.53	**≤ -68.56**
Worst Other Spur [dBc]	**≤ -67.03**	≤ -66.83
Spurious Free Dynamic Range [dBc]	≥ 66.53	**≥ 66.83**
ENOB [bits]	≥ 7.876	**≥ 7.896**
Cross-Talk [dBc]	**≤ -65.69**	≤ -61
IP3 [dB] (F1=184.7 MHz; F2=187.5 MHz)	29.55	**32.2**
IP2 [dB] (F1=184.7 MHz; F2=187.5 MHz)	66.3	**77.5**
Fs: 700 MSPS --- BW: 375 ÷ 650 MHz		
ADC Performance Parameters	**ADU Board#1 (with ADA)**	**ADU Board#2 (without ADA)**
Signal to Noise Ratio referenced to Full Scale [dBFS]	≥ 48.88	**≥ 49.32**
Gain Flatness [dBFS]	**≤ ±0.6252**	≤ ±1.356
2nd-order Harmonic Distortion [dBc]	**≤ -65.77**	≤ -59.9
3rd-order Harmonic Distortion [dBc]	≤ -60.78	**≤ -65.64**
Worst Other Spur [dBc]	**≤ -64.16**	≤ -63.23
Spurious Free Dynamic Range [dBc]	**≥ 60.78**	≥ 59.9
ENOB [bits]	≥ 7.788	**≥ 7.886**
Cross-Talk [dBc]	**≤ -70.58**	≤ -70.39
IP3 [dB] (F1=500.1 MHz; F2=503.2 MHz)	**26**	24.4
IP2 [dB] (F1=500.1 MHz; F2=503.2 MHz)	**64**	58.3

Table 7: Comparison of the two ADU Boards in terms of performance parameters.

Note that the values reported in the table are relative to the worst case: that is the worst value considering all ADU inputs and all frequencies for that particular measurement. Also we have highlighted with bold type the best value between the two boards.
Looking at these results, the first consideration is that there are not so remarkable differences, probably except for gain flatness in the high frequency band. But this aspect could make the ADU board with ADA more preferable than the other one in high frequencies.
On the other hand, considering the low frequency band the ADU board without ADA seems to work slightly better.

7 References

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Perini, F., Rusticelli, S., Monari, J., & Schiaffino, M. (2015). *Report on WDM RFoF Solution.* Low Frequency Aperture Array, SKA-TEL-LFAA-0400022-RX-AST-R-01C.

8 APPENDIX A – ADC Memory Map Register Table

As previously said, the CPLD is dedicated to the management of the board and provides the communication between the host computer and all the onboard chips through the Gigabit Ethernet link. Every chip is mapped into the CPLD that forwards SPI and I2C requests and acknowledgements.
Each row in the memory map register table has eight bit locations. The memory map is divided into four sections: the Analog Devices SPI registers (Register 0x000 to Register 0x00D), the analog input buffer control registers, the ADC function registers, the DDC function registers and finally the digital outputs and test modes registers.
During the ADU bootstrap all the registers listed in Table 8 are configured.

Reg Addr (Hex)	**Register Name**	**Bit 7 (MSB)**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0 (LSB)**	**Default**	**Notes**
Analog Devices SPI Registers											
0x000	INTERFACE_ CONFIG_A	Soft reset (self clearing)	LSB first 0 = MSB 1 = LSB	Address ascension	0	0	Address ascension	LSB first 0 = MSB 1 = LSB	Soft reset (self clearing)	0x00	
0x001	INTERFACE_ CONFIG_B	Single instruction	0	0	0	0	0	Datapath soft reset (self clearing)	0	0x00	
0x002	DEVICE_ CONFIG (local)	0	0	0	0	0	0	00 = normal operation 10 = standby 11 = power-down		0x00	
0x003	CHIP_TYPE	011 = high speed ADC								0x03	Read only
0x004	CHIP_ID (low byte)	1	1	0	0	0	1	0	1	0xC5	Read only
0x005	CHIP_ID (high byte)	0	0	0	0	0	0	0	0	0x00	Read only
0x006	CHIP_ GRADE	1100 = 1250 MSPS 1010 = 1000 MSPS 1000 = 820 MSPS 0101 = 500 MSPS				X	X	X	X		Read only
0x008	Device index	0	0	0	0	0	0	Channel B	Channel A	0x0	
0x00A	Scratch pad	0	0	0	0	0	0	0	0	0x00	
0x00B	SPI revision	0	0	0	0	0	0	0	1	0x01	
0x00C	Vendor ID (low byte)	0	1	0	1	0	1	1	0	0x56	Read only
Reg Addr (Hex)	**Register Name**	**Bit 7 (MSB)**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0 (LSB)**	**Default**	**Notes**
0x00D	Vendor ID (high byte)	0	0	0	0	0	1	0	0	0x04	Read only
Analog Input Buffer Control Registers											
0x015	Analog input (local)	0	0	0	0	0	0	0	Input disable 0 = normal operation 1 = input disabled	0x00	

0x016	Input termination (local)	Analog input differential termination 0000 = 400 Ω(default) 0001 = 200 Ω0010 = 100 Ω0110 = 50 Ω				1110 = AD9680-1250 and AD9680-1000 1100 = AD9680-820 and AD9680-500				0x0E for AD9680-1250 and AD9680-1000; 0x0C for AD9680-820 and AD9680-500	
0x934	Input capacitance (local)	0	0	0	0x1F = 3 pF to GND (default) 0x00 = 1.5 pF to GND					0x1F	
0x018	Buffer Control 1 (local)	0000 = 1.0× buffer current 0001 = 1.5× buffer current 0010 = 2.0× buffer current (default for AD9680-500) 0011 = 2.5× buffer current 0100 = 3.0× buffer current (default for AD9680-1000 and AD9680-820) 0101 = 3.5× buffer current (default for AD9680-1250) … 1111 = 8.5× buffer current				0	0	0	0	0x50 for AD9680-1250; 0x40 for AD9680-1000 and AD9680-820; 0x20 for AD9680-500	
0x025	Input full-scale range (local)	0	0	0	0	Full-scale adjust 0000 = 1.94 V 1000 = 1.46 V 1001 = 1.58 V (default for AD9680-1250) 1010 = 1.70 V (default for AD9680-1000 and AD9680-820) 1011 = 1.82 V 1100 = 2.06 V (default for AD9680-500)				0x09 for AD9680-1250; 0x0A for AD9680-1000 and AD9680-820; 0x0C for AD9680-500	V p-p differential; use in conjunction with Reg. 0x030
0x030	Input full-scale control (local)	0	0	0				0	0		Used in conjunction with Reg. 0x025
Digital Outputs and Test Modes											
0x550	ADC test modes (local)	User pattern selection 0 = continuous repeat 1 = single pattern	0	Reset PN long gen 0 = long PN enable 1 = long PN reset	Reset PN short gen 0 = short PN enable 1 = short PN reset	Test mode selection 0000 = off, normal operation 0001 = midscale short 0010 = positive full scale 0011 = negative full scale 0100 = alternating checker board 0101 = PN sequence, long 0110 = PN sequence, short 0111 = 1/0 word toggle 1000 = the user pattern test mode (used with Register 0x0550, Bit 7 and User Pattern 1 to User Pattern 4 registers) 1111 = ramp output				0x00	
0x564	Output channel select	0	0	0	0	0	0	0	Converter channel swap 0 = normal channel ordering 1 = channel swap enabled	0x00	
0x56E	JESD204B lane rate control	0	0	0	0 = serial lane rate ≥6.25	0	0	0	0	0x00 for AD9680-1250, AD9680-1000 and	

					Gbps and ≤12.5 Gbps 1 = serial lane rate must be ≥ 3.125 Gbps and ≤6.25 Gbps					AD9680-820; 0x10 for AD9680-500	
Reg Addr (Hex)	**Register Name**	**Bit 7 (MSB)**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0 (LSB)**	**Default**	**Notes**
0x56F	JESD204B PLL lock status	PLL lock 0 = not locked 1 = locked	0	0	0	0	0	0	0	0x00	Read only
0x570	JESD204B quick config-uration	JESD204B quick configuration L = number of lanes = $2^{\text{Register 0x570, Bits[7:6]}}$ M = number of converters = $2^{\text{Register 0x570, Bits[5:3]}}$ F = number of octets/frame = $2^{\text{Register 0x570, Bits[2:0]}}$								0x88 for AD9680-1250, AD9680-1000 and AD9680-820; 0x49 for AD9680-500	Refer to DataSheet Table 26 and Table 27
0x58B	JESD204B parameters SCR/L	JESD204B scrambling (SCR) 0 = disabled 1 = enabled	0	0	0	0	0	JESD204B lanes (L) 00 = 1 lane 01 = 2 lanes 11 = 4 lanes Read only, see Register 0x570		0x8X	
0x58C	JESD204B F config	Number of octets per frame, F = Register 0x58C[7:0] + 1								0x88	Read only, see Reg. 0x570
0x58D	JESD204B K config	0	0	0	Number of frames per multiframe, K = Register 0x58D[4:0] + 1 Only values where (F × K) mod 4 = 0 are supported					0x1F	See Reg. 0x570
0x58E	JESD204B M config	Number of Converters per Link[7:0] 0x00 = link connected to one virtual converter (M = 1) 0x01 = link connected to two virtual converters (M = 2) 0x03 = link connected to four virtual converters (M = 4) 0x07 = link connected to eight virtual converters (M = 8)									Read only
0x58F	JESD204B CS/N config	Number of control bits (CS) per sample 00 = no control bits (CS = 0) 01 = 1 control bit (CS = 1); Control Bit 2 only 10 = 2 control bits (CS = 2); Control Bit 2 and 1 only 11 = 3 control bits (CS = 3); all control bits (2, 1, 0)		0	ADC converter resolution (N) 0x06 = 7-bit resolution 0x07 = 8-bit resolution 0x08 = 9-bit resolution 0x09 = 10-bit resolution 0x0A = 11-bit resolution 0x0B = 12-bit resolution 0x0C = 13-bit resolution 0x0D = 14-bit resolution 0x0E = 15-bit resolution 0x0F = 16-bit resolution					0x0F	
Reg Addr (Hex)	**Register Name**	**Bit 7 (MSB)**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0 (LSB)**	**Default**	**Notes**
0x590	JESD204B N' config	0	0	Subclass support (Subclass V) 0 = Subclass 0 (no deter-ministic	ADC number of bits per sample (N') 0x7 = 8 bits 0xF = 16 bits					0x2F	

				latency) 1 = Subclass 1			
0x591	JESD204B S config	0	0	1	Samples per converter frame cycle (S) S value = Register 0x591[4:0] + 1	0x20	Read only

Table 8: ADC memory map registers configured during the ADU bootstrap.

9 APPENDIX B – Lab RFI Monitoring

Since the ADU board is unshielded an RFI monitoring campaign of the laboratory was performed in order to make sure that the board was not affect by the test environment.

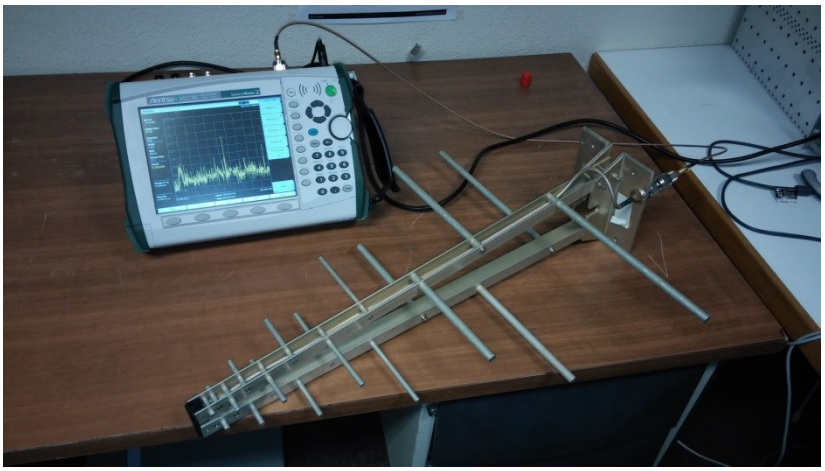

Figure 41: Equipment used for RFI measurement.

The highest RFI is at 378 MHz and it is generated by a local oscillator in the receiver rack of the Northern Cross Radio Telescope. The next highest RFI is 16 dB lower at 625 MHz.

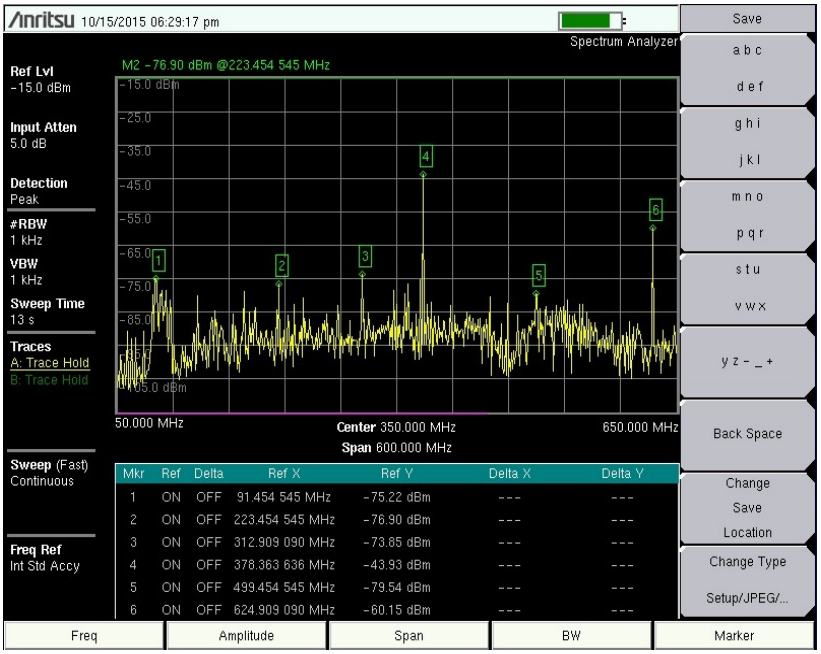

Figure 42: The highest RFI measured with spectrum analyzer (Peak Detection mode).

Once identified, the sources of the strongest RFI were switched off during the measurement session. So we had the certainty that the FFT power spectrum, used to calculate evaluation parameters, took into consideration only harmonic distortion products and spurious signals generated internally in the board.