Mem. S.A.It. Vol. 75, 282

Memorie della

Programmable fast data acquisition system

S. Montebugnoli, G. Bianchi, L. Zoni

INAF – Istituto di Radioastronomia, Via P.Gobetti 101, I-40129 Bologna

Abstract. The goal of this work is to investigate the possibility to install on modern radiotelescopes a fast and programmable backend instead of several backends, each dedicated to single acquisition task. Such an approach could lower the costs and make available a more compact and flexible back end. Exploiting the state-of-the-art of the FPGAs (Field Programmable Gate Arrays) and innovative architectures, a programmable system might be conceived.

1. Introduction

Modern radiotelescopes, such as the SRT (Sardinia Radio Telescope), could take advantage from state-of-the-art fast data acquisition systems. Up to now each experiment has exploited a dedicated backend, and what we want to investigate here is the possibility to design a single digital programmable system that can satisfy any observational requirement.

In Fig. 1 we show the concept on which the planned system is based. The number of quantization levels of the analog-to-digital conversion block will be determined on the base of the presence of radio frequency interferences (RFIs) within the band. The dynamic range of the A/D can span from 2 bit (12 dB) to 14 bit (96 dB). The sizing of the A/D word length is programmed through the resizing (Resc.) block, while the algorithms used in the processing phase are programmed in the Pps (Programmable processing system). In principle such a system can fit the requirements of the major part of the processing algorithms only if the processing power of the Pps block is large enough. Therefore the Pps must offer the largest computation power nowadays available.

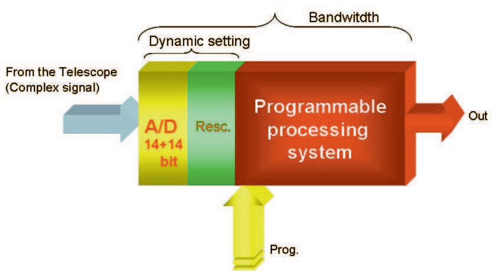

Fig. 1. Basic block diagram.

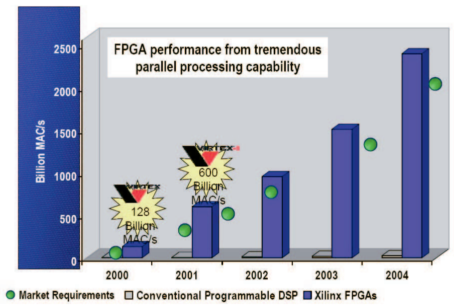

Fig. 2. Performances in parallel computation.

2. The system

We have just mentioned the very high computation power requested by the Pps in order to face any post-processing demand. The challenge is how to obtain it. The idea is to exploit the speed of the hardware and the flexibility of the software offered by the FPGA.
In Fig. 2 the increase in the FPGA's performance over the last 5 years, due to the parallel processing capability of FPGA, is clearly visible.
From the same figure it is also clear that the DSPs performance evolution did not follow, in practice, the computation power related to the market requirements. The general block diagram of the programmable fast data acquisition system and a pictorial view of a possible layout of the board are visible in Figs. 3 and 4. The plan is to implement a double system, one on each side of the same board (power dissipation levels are under investigation) but here we describe the single system. A 100-MHz complex signal (I,Q) is expected to be supplied from the base band converter of the radiotelescope. The analog-to-digital conversion stage is based on a wide band (105 MS/sec) and very wide dynamic range (14 bit) A/D (Analog device AD 6645). The digital word is sent to the FPGA # 1 where it is rescaled to the proper word length to obtain the minimum requested dynamic range (correlated with the RFI's environment) and to reduce as much as possible the amount of data to be handled. Through the FPGA # 2 it is possible to send data directly to the PC (via the PCI bridge) if a time domain processing is requested. The FPGA # 1 is programmed to obtain a polyphase filter bank (up to 64k channels). An averaged power spectrum (the integration time can be programmed) is available through the FPGA # 4. In this way a 100-MHz input bandwidth real-time spectrometer can be implemented. The complex spectrum is sent to the CTM (Corner Turn Memory). The CTM and the FPGA # 2 are the core of the high-resolution side of the same spectrometer. Spectra are entered into the CTM by rows while the FFT (FPGA # <2) are computed by columns (i.e., if we have 16k rows and 16k columns, a 256 Mchannels high-resolution spectrometer is available).

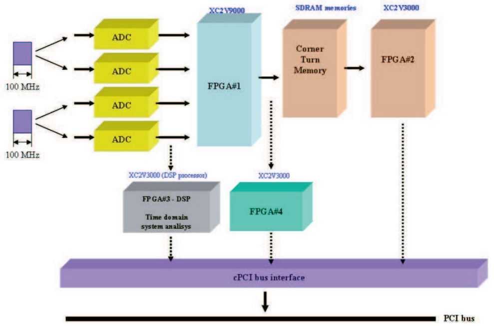

Fig. 3. Complete block diagram.

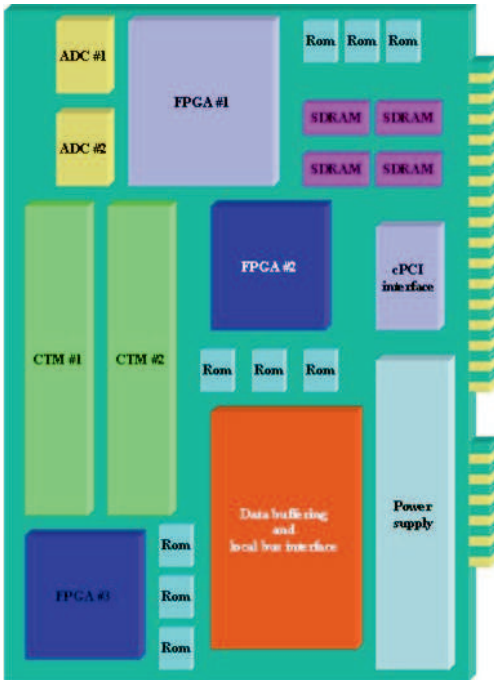

Fig. 4. Theorical layout.

In other words, all the FPGAs blocks can be optimized and programmed to obtain the desired task as:

- High resolution spectroscopy: 0.256–64 kchannels each module (16+16 bit) BW=100 MHz.
- Polarimetry: potentially a 100-MHz band can be analyzed.
- Ultra-High resolution spectroscopy: 256 million channels in real time + Serendip-like data processing.
- Time-domain analysis: (Karhunen-Loeve Transform, SSA etc. etc.)

In order to maintain a low risk profile in the design and gain at the same time experience in the FPGAs programming, a PCI subsystem board (composed only by the A/Ds and the FPGA # 1) has been designed and is under test now. A 3.000.000-gates Xilinx Virtex-II family FPGA (XC2V3000) has been used in this evaluation prototype along with a PCI bridge. A Polyphase Filter Bank (PFB) is under implementation in this FPGA in order to test a first level of software and data transmission from the board to the PC. In Fig. 5 a picture of the prototype being tested is shown.
If the test of the VIIP board is successful, the more complicated layout of the overall system board (schematized in Fig. 4) will be faced.

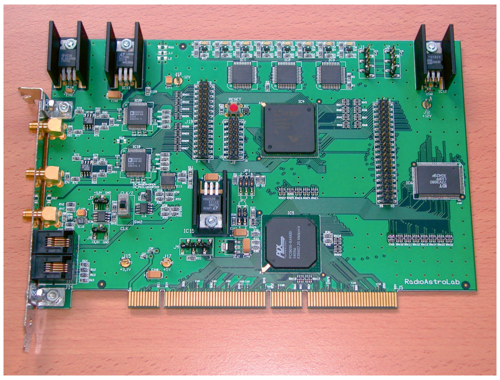

Fig. 5. VIIP Prototype board.

3. Conclusion

A programmable fast data acquisition system is under design at the Medicina radiotelescope labs. Such a system could represent an innovative approach to the backend design able to reduce costs, space and, due to its very high on-line computation power, increase flexibility for different applications. This might also be useful as a platform to test new on-line processing algorithms.