Nov 20, 2002

HPRI-CT-2001-50031 "FARADAY"
Subproject 2: 22GHz receiver array First Year Report
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IRA Reference document: Specification_1.doc

Task schedules and status:

Months 1-7: Start-up phase

- Recruit microwave engineer

Status:
Dr. Andrea Cremonini is full time working on the project as microwave engineer. Owing to the difficulties encountered by JBO in the recruitment of a microwave engineer, Cremonini has assumed most of the LNAs design activity which was originally planned under JBO responsibility for subproject 2. The activity includes also the direct interaction with CSIRO with several periods of work in Australia.

- Initial design study with other partners to investigate the current state-of-the art for MMIC design processes and software, establish overall design criteria and specifications, select candidate foundries fro production of MMIC wafers

Status:
This task was fully covered by meetings, telecons attended by Cremonini, Orfei and Tofani and by a period of 15 days at CSIRO (AUS) by Cremonini. The agreement signed by IRA with CSIRO and later with TRW allowed IRA to get the software needed for the LNA design with TRW InP technology. Also with the cooperation with CSIRO, JBO and ASTRON, IRA has produced the design of 4 LNAs for the bandwidth 18-26 GHz (a specification larger than the planned one). Three of these layouts will be adopted for the first foundry run after the next period of work of Cremonini at CSIRO by the end of November 2002.

- Electromagnetic design of the passive receiver components

Status:
As assumed in the project plan, this activity was carried out in cooperation with MECSA (I) with the delivery of the design of a variable profile corrugated horn with top performances. The design allowed to have the feed horn included in the dewar, improving the receiver sensitivity. The design of a broadband polarizer with OMT has been carried out at a lower band (6-8 GHz) and wil be used for a scaled version in the band of FARADAY.

- Mechanical design of the cryogenic system

Status:
A dewar with plane surfaces which gives better space for the five horn array has been designed in Florence. It includes also the possibility to accomodate all the microwave components of the receiver and it accounts for the planned power dissipation of the active components.

Months 7-15: Start of receiver construction

- Construction of feed horns, polarizers and ortho-mode transitions

Status:
Five corrugated horns have been built and tested. One prototype polarizer/OMT at lower frequency band has been built and tested.

- Construction of the cryogenic system

Status:
The dewar has been built and feedhorns were mounted inside. Various tests were performed on the cooling performances of the system. Work is still going on for the optical windows and for the passive component mounts.

1. LNA

The amplifier needed for the subproject 2 originally had the following requirements:

- Center frequency 22 GHz
- Bandwidth goal 18-26 GHz (Faraday specs 21-26 GHz may be improved)
- Gain up to 36 dB
- Optimised noise temperature < 20 K when operating at T=20K

More requirements can be the input return loss and the intermodulation level at the output of the LNA. The former is highly dependent on the noise optimisation. An ideal LNA should have minimum input noise with a reasonably high return loss (say at least 15 dB). In any case since noise temperature optimisation has the top priority for the first stage we may think about the use of isolators.
Cryogenic isolators suitable for this design are commercially available and their losses are compatible with the noise specs [2]. If needed, the waveguide isolator is more suitable with respect to the stripline circulator. The waveguide component although more critical to thermal stresses, has been tested in many cryogenic systems and can be purchased on the market. The only problem could be a selection among components since the performance at cryogenic temperature may vary mainly on the bandwidth. Expected insertion losses are of the order of 0.5 dB thus introducing only few K in the receiver noise temperature.
The experience gained on hybrid LNAs, developed by NRAO on InP 0.1micron technology for space projects such as Sport and Cassini [1], put a limit on the achieved gain of about 36 dB. Above this level, problems of saturation, oscillation or intermodulation may occur [2] and IP3 turns out to be very low.
A MMIC realization of the LNAs to be made within the Faraday context put also a constraint in the dimensions of the chip area (see wafer analysis in section 3) at a level of 7 mm^2, and this means a limit on the number of amplifier stages and thus on gain. Crossing together this constraint with IP3 level and noise request an alternative design has been followed in subproject 2: the cold part of the amplification chain will be made by two amplifiers, one optimized for noise with a gain of 26dB (LNA1), the other one optimized for IP3 with a gain of 20dB (LNA2, fig. 1). 26 dB of gain are enough to mask the noise of the isolator plus the 20dB gain LNA noise and their cascade masks the total noise coming from the IF part of the receiver.
The design of the amplifiers have been realized using the software package LIBRA Series IV, under which the libraries of the circuit components (agreement with TRW) and the relative layout macros (agreement with CSIRO) are available. The starting philosophy of the circuit takes experience from the already done devices designed and constructed by CSIRO and around it five different designs were made for the LNA1. Three designs use a polarization current of the HEMTs equal to 60%Idss (LNA1_01, LNA1_04, LNA1_05) in order to get a compromise between low power consumption (100%Idss has been avoided for this reason) and noise performance (10%Idss gives minimum noise but very sensitive to current fluctuations). The other two designs (LNA1_02, LNA1_03) were based on 10%Idss biasing current model, but they will not be considered because the information about noise model are too poor and the final result could be too much unpredictable. Due to the few information about the behaviour of the cooled HEMT used at Idss biasing current other than 60% we thought to be conservative, using the same CSIRO approach. After the chip will be produced, at the moment of the measurement stage, we will tune the bias current and voltage stage by stage to obtain the best performances. So in the final stage of the design only three of five have been considered remarkable: a conservative design (LNA1_01), where straight transmission lines only are used, a mix design (LNA01_04), where the input network is made by using distributed and concentrated components and an enhanced LNA01_04, named LNA01_05, where the isolation

from the different biasing pads, that could be source of oscillation, and the gain flatness have been improved.

In the following, simulated performance of the LNA1, both for design version 1 and 4, are reported. Version 4 has better performance in term of noise and use straight line and a lumped inductor to connect input stage. Version 1 uses instead a bent line and shows worst noise. A summary of performances is

- 3 stages amplifier
- Gain = 25.5dB ± 1dB over the 18-26GHz band , Version 1 and 4; 25.6dB –0.3dB Version 5
- Input an output return loss < -10dB over the band. Much better values are obtained in the restricted band 21-26GHz, particularly in the Version 5.
- Noise = 90÷100 K over the band Version 4; 110÷130K Version 1, 89÷97K Version 5 (at ambient temperature)
- chip dimension = 7.2 mm^2
- max power consumption ≈ 85mW

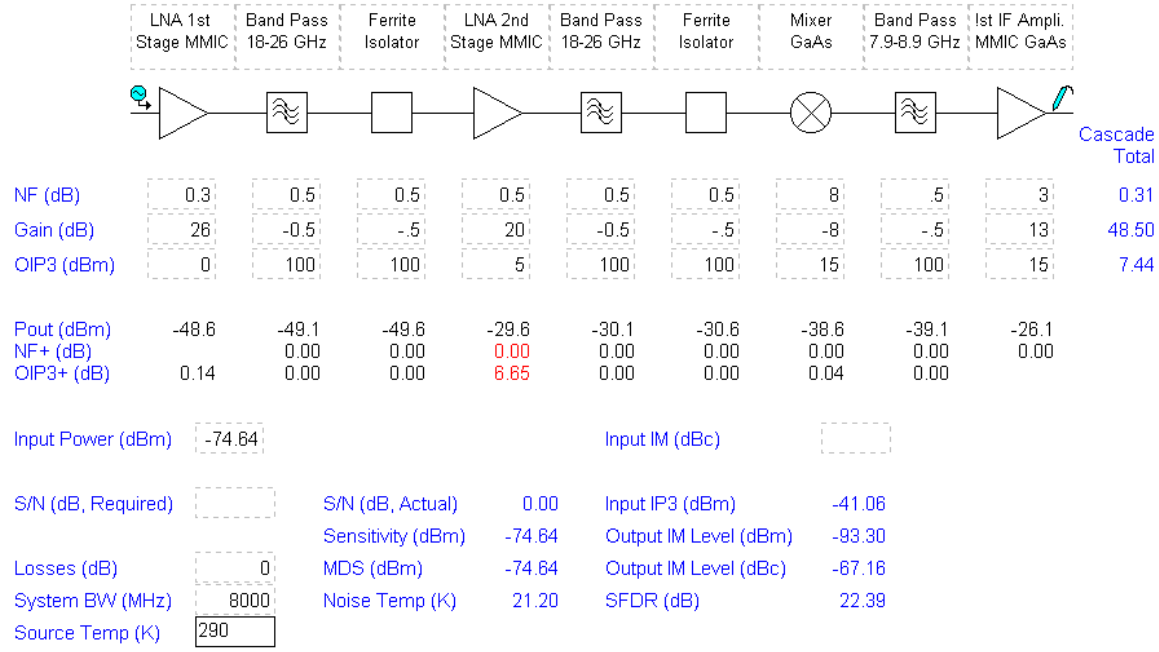


Fig. 1 Receiver configuration

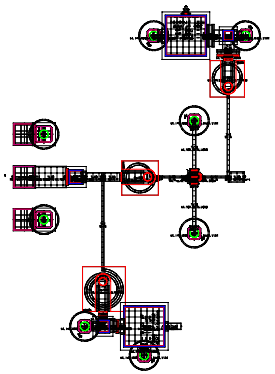
FET Breakdown considerations - The ohmic value of the drain bias network must be carefully considered in order to reduce the possibility to damage the HEMT because of the breakdown voltage. From CSIRO experience a breakdown voltage within the range 1.6 to 2 Volt could be defined. These LNAs were designed with Vds=0.9 V and Ids=18 mA and assuming that the breakdown voltage is 1.6 V.
40 Ω was fixed as the maximum resistance value on the drain bias network. With this value Vd will be 1.6V, and the voltage drop on the resistors will be 0.7 V with Ids=18mA. One can reduce the Ids value down to 5mA, don't changing the Vd value, without damage the device (Vds become 1.4 V and the voltage drop on the resistors 0.2V).
This protection is important especially when the device is turned on and for reducing the possibility of device damage during the bias optimization.

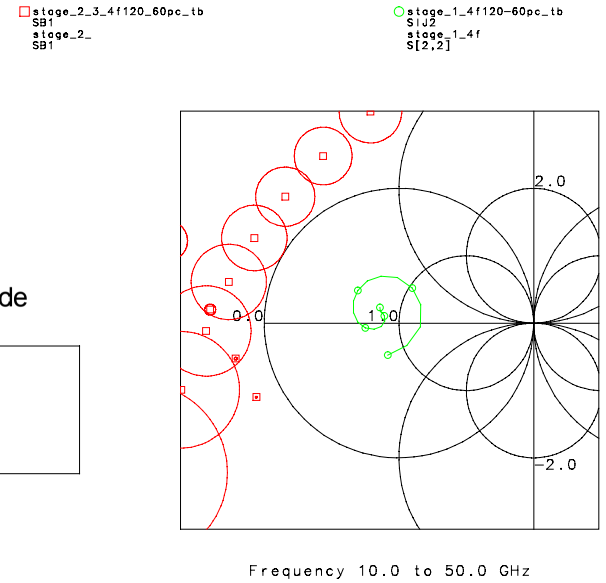
Power Dissipation - The TRW HEMT are noise modelled for 60%Idss bias only. For this reason the device is designed with a DC power consumption of about 29 mW per stage, calculated with Vds=0.9 Ids=18mA Rdmax=40 Ω. **(**Note that with Ids=5mA the DC power consumption decrease down to 5.5 mW)

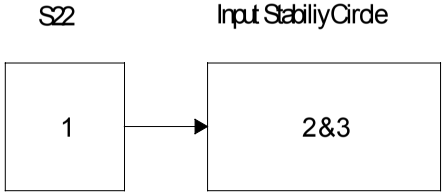
Low Noise Amplifier 18 to 26 GHz, Version 4 (November 6, 2002)

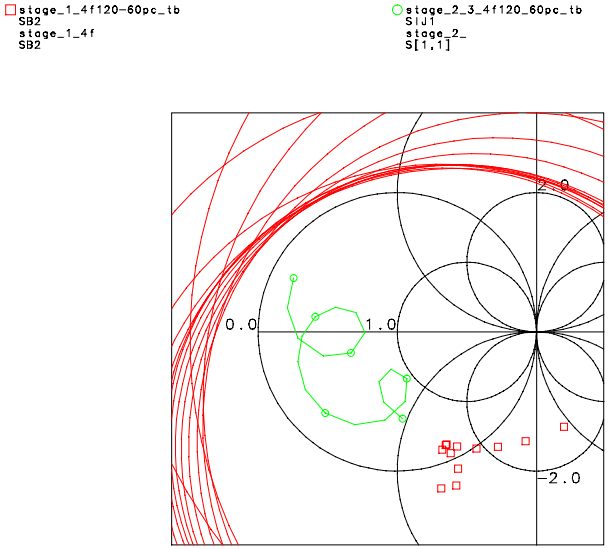
Three stage 0.9 Vds 18 mA Ids

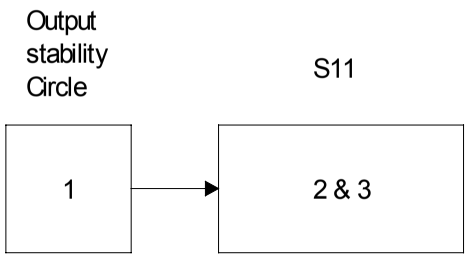
Stability stage description

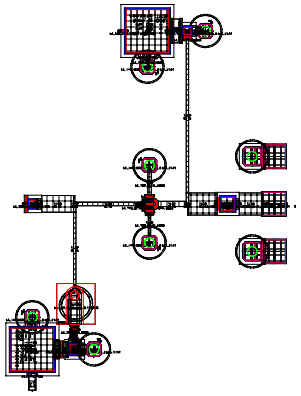






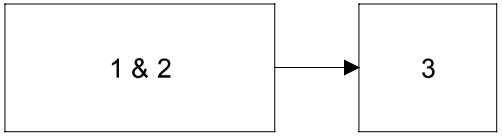


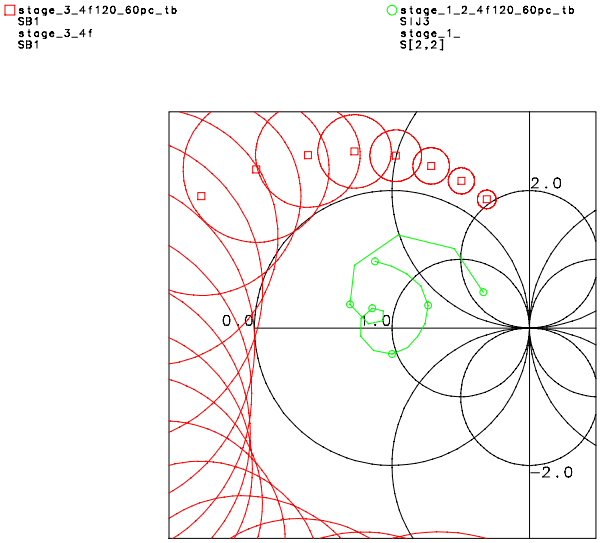




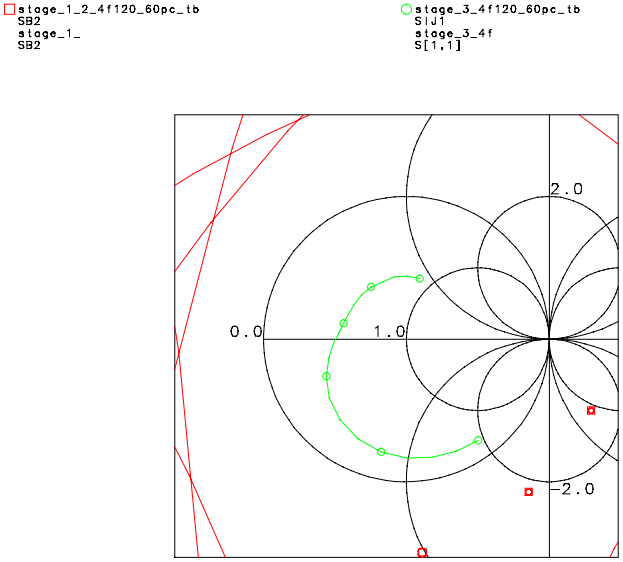
S22

Input stability Circle





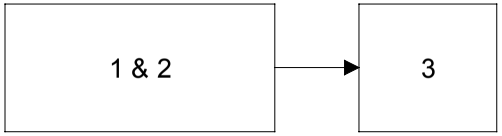
Frequency 10.0 to 50.0 GHz

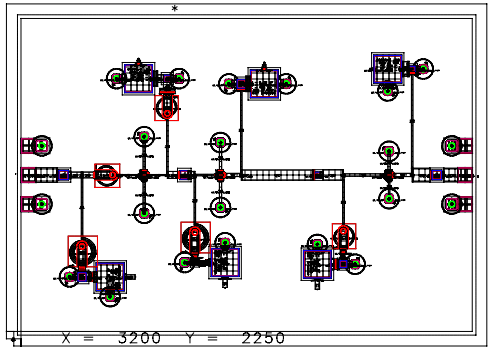


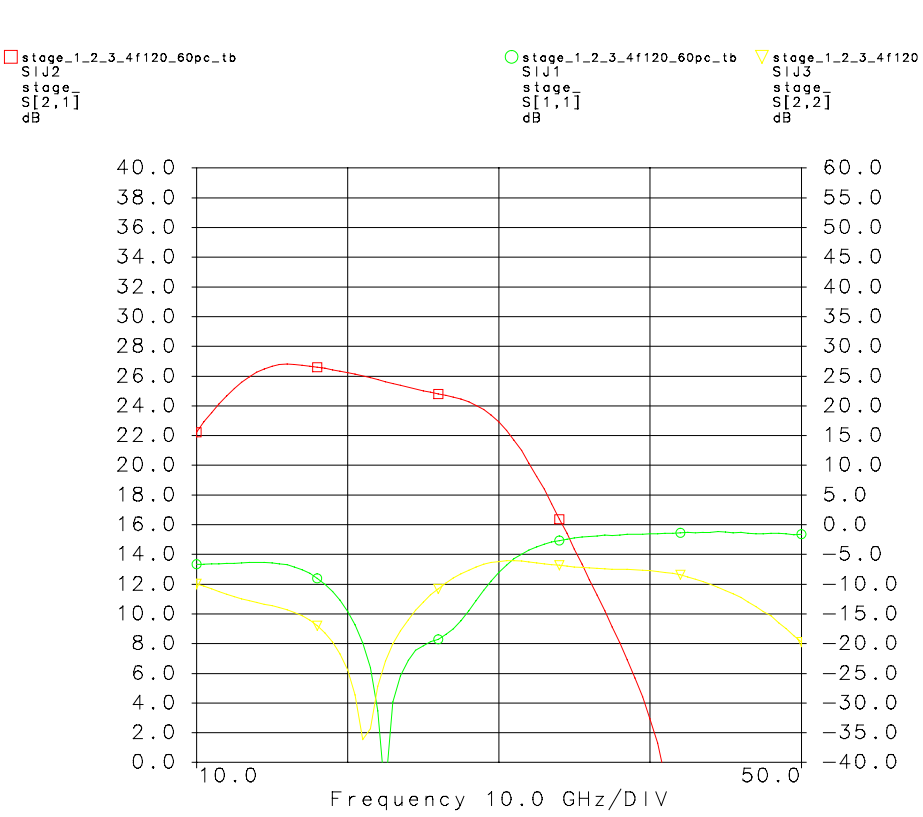
Frequency 10.0 to 50.0 GHz

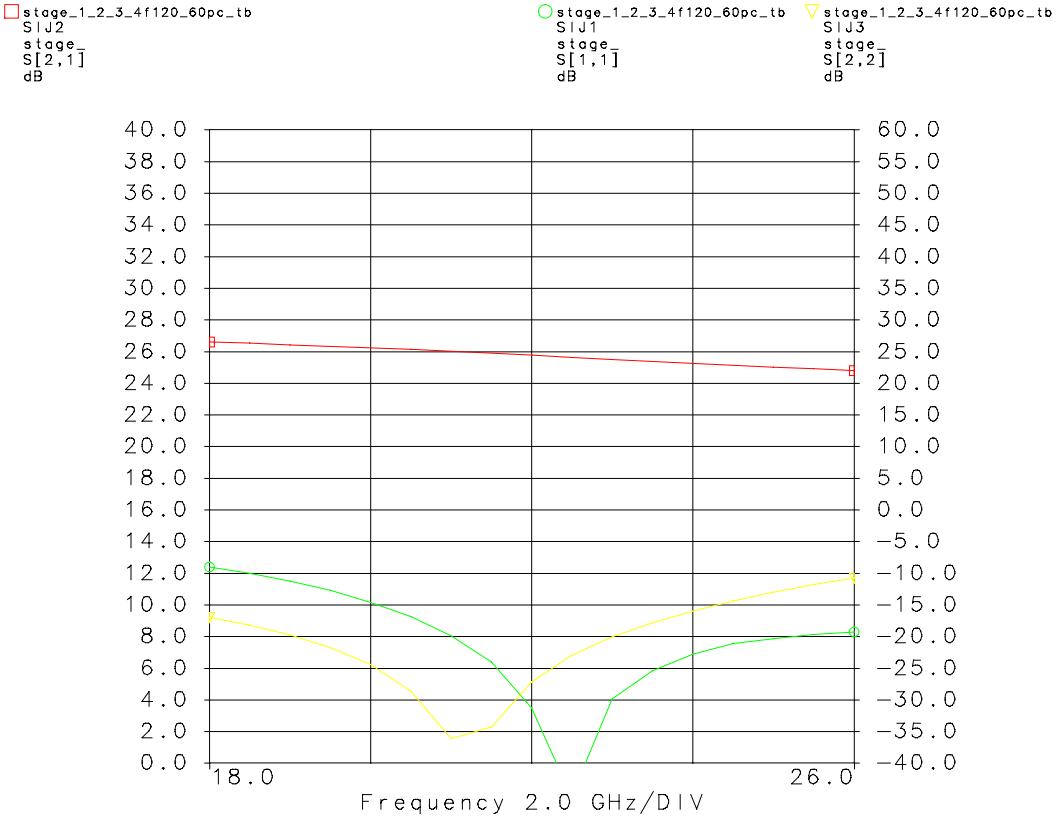
Output Stability Circle

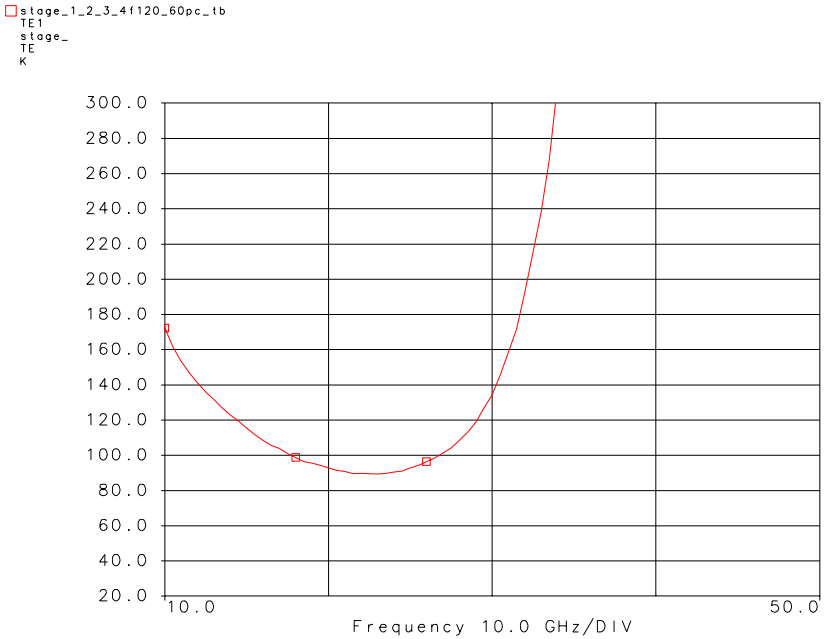
S11

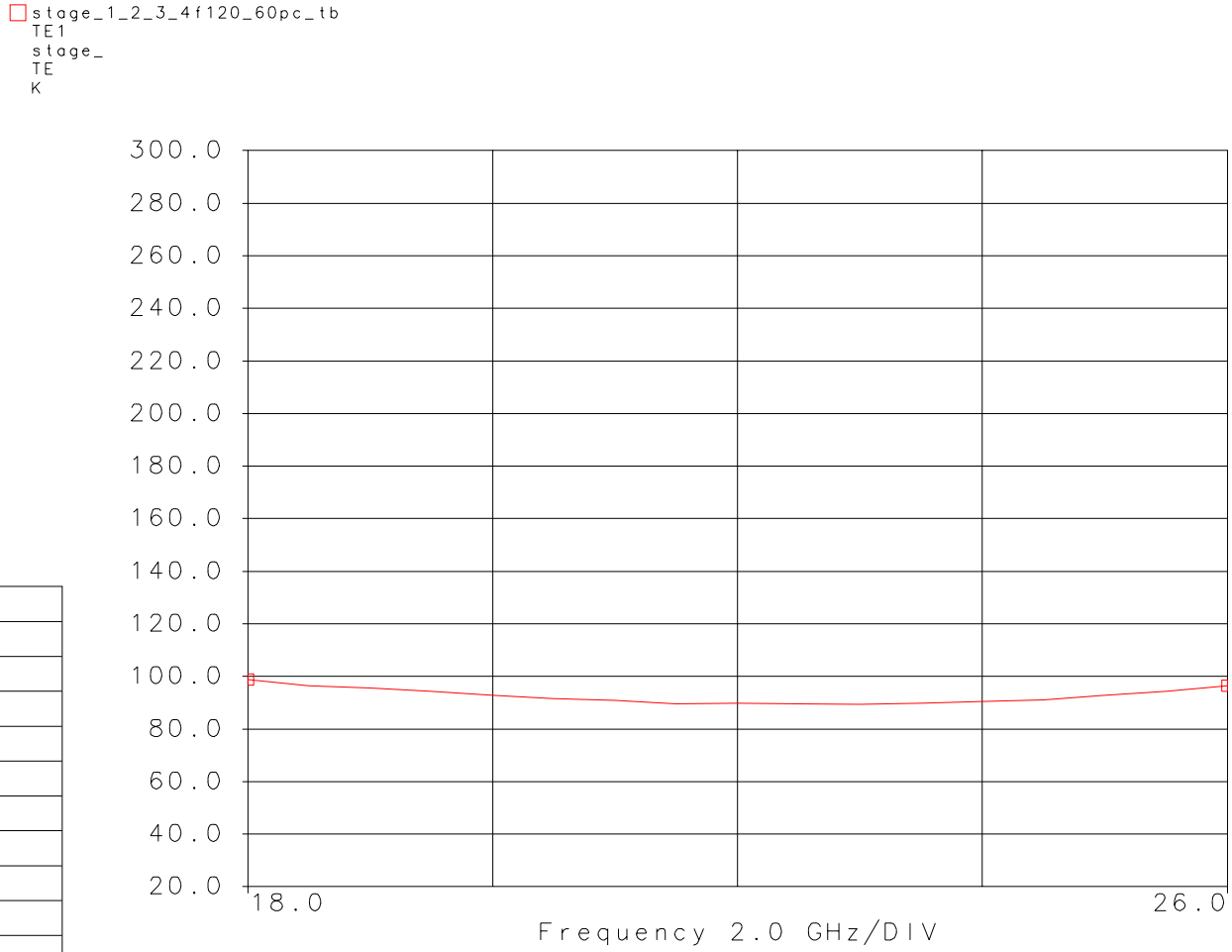



X = 3200 Y = 2250


stage_1_2_3_4f120_60pc_tb
SIJ2
stage_
S[2,1]
dB
stage_1_2_3_4f120_60pc_tb
SIJ1
stage_
S[1,1]
dB
stage_1_2_3_4f120
SIJ3
stage_
S[2,2]
dB
40.0
38.0
36.0
34.0
32.0
30.0
28.0
26.0
24.0
22.0
20.0
18.0
16.0
14.0
12.0
10.0
8.0
6.0
4.0
2.0
0.0
60.0
55.0
50.0
45.0
40.0
35.0
30.0
25.0
20.0
15.0
10.0
5.0
0.0
-5.0
-10.0
-15.0
-20.0
-25.0
-30.0
-35.0
-40.0
10.0
50.0
Frequency 10.0 GHz/DIV


stage_1_2_3_4f120_60pc_tb
SIJ2
stage_
S[2,1]
dB
stage_1_2_3_4f120_60pc_tb
SIJ1
stage_
S[1,1]
dB
stage_1_2_3_4f120_60pc_tb
SIJ3
stage_
S[2,2]
dB
40.0
38.0
36.0
34.0
32.0
30.0
28.0
26.0
24.0
22.0
20.0
18.0
16.0
14.0
12.0
10.0
8.0
6.0
4.0
2.0
0.0
60.0
55.0
50.0
45.0
40.0
35.0
30.0
25.0
20.0
15.0
10.0
5.0
0.0
-5.0
-10.0
-15.0
-20.0
-25.0
-30.0
-35.0
-40.0
18.0
26.0
Frequency 2.0 GHz/DIV


stage_1_2_3_4f120_60pc_tb
TE1
stage_
TE
K
300.0
280.0
260.0
240.0
220.0
200.0
180.0
160.0
140.0
120.0
100.0
80.0
60.0
40.0
20.0
10.0
50.0
Frequency 10.0 GHz/DIV

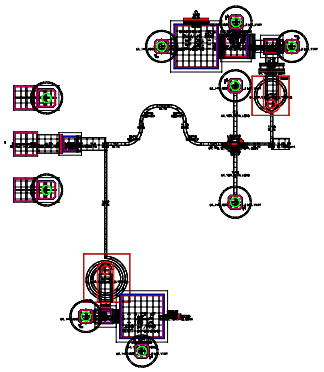

stage_1_2_3_4f120_60pc_tb
TE1
stage_
TE
K
300.0
280.0
260.0
240.0
220.0
200.0
180.0
160.0
140.0
120.0
100.0
80.0
60.0
40.0
20.0
18.0
26.0
Frequency 2.0 GHz/DIV

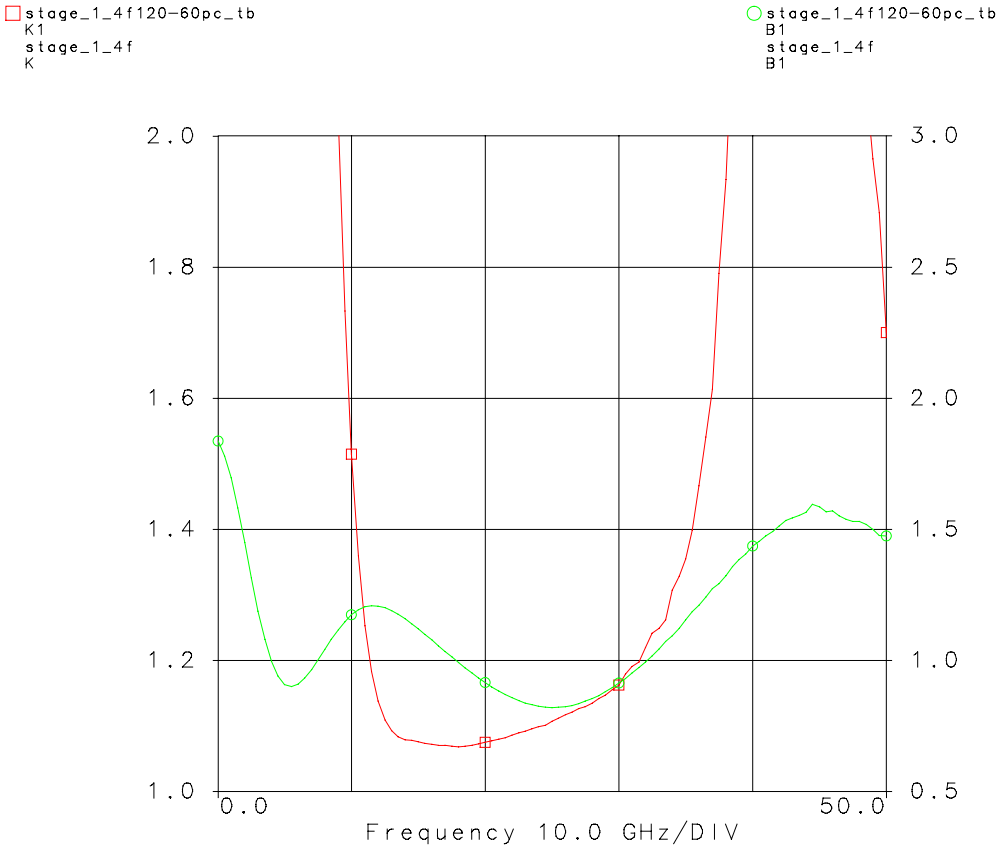
Low Noise Amplifier 18 to 26 GHz Version 1 (November 6, 2002)

Three stage 0.9 Vds 18 mA Idss

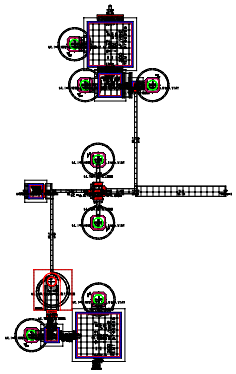
Stability stage description

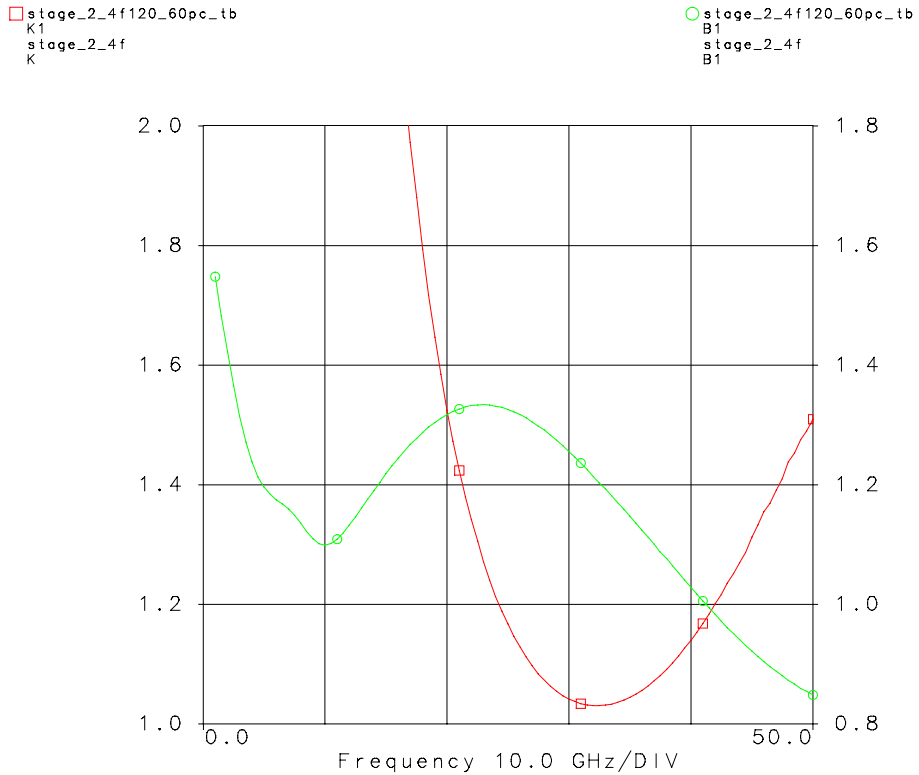
Stage 1



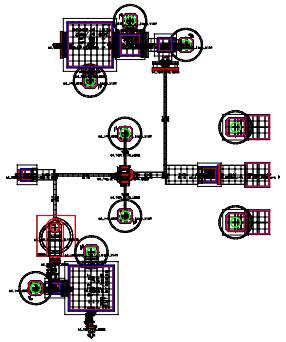


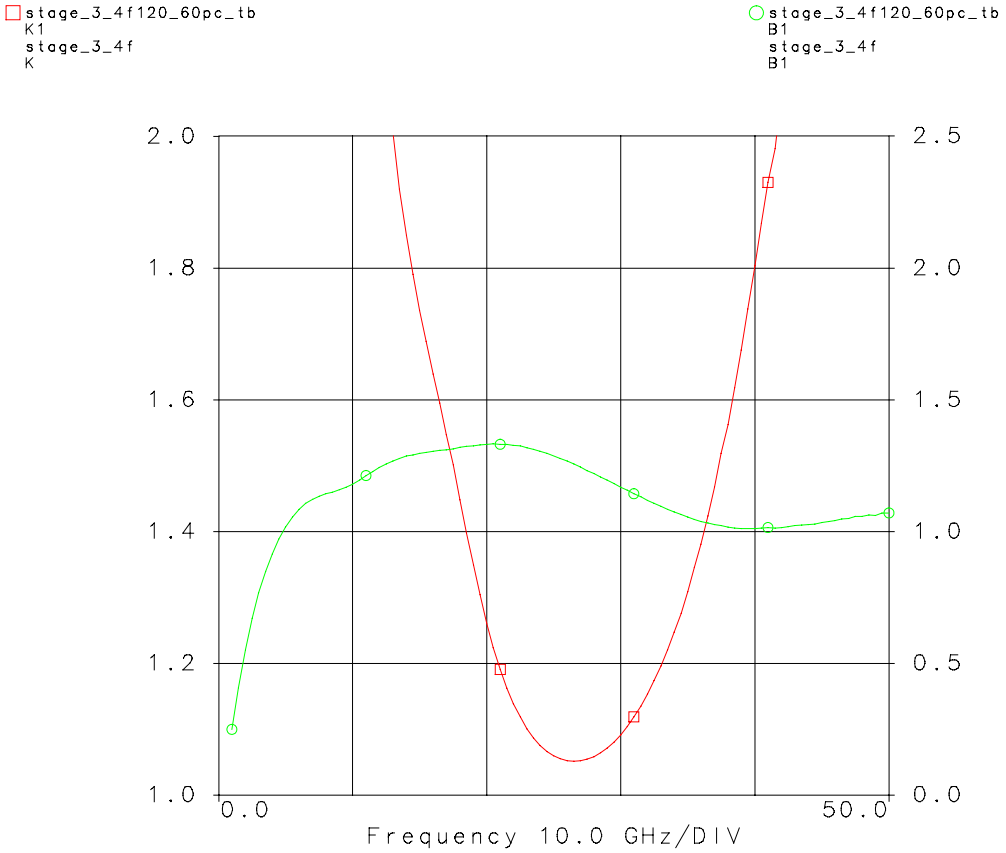
Stage 2




stage_2_4f120_60pc_tb
K1
stage_2_4f
K
stage_2_4f120_60pc_tb
B1
stage_2_4f
B1
2.0
1.8
1.6
1.4
1.2
1.0
1.8
1.6
1.4
1.2
1.0
0.8
0.0
50.0
Frequency 10.0 GHz/DIV

Stage 3

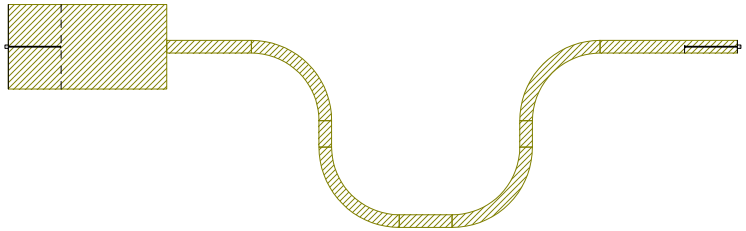



stage_3_4f120_60pc_tb
K1
stage_3_4f
K
stage_3_4f120_60pc_tb
B1
stage_3_4f
B1
2.0
1.8
1.6
1.4
1.2
1.0
2.5
2.0
1.5
1.0
0.5
0.0
0.0
50.0
Frequency 10.0 GHz/DIV

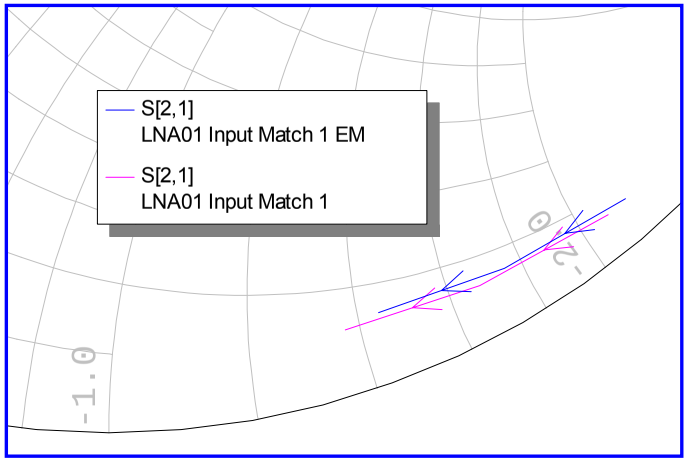
EM SIMULATION OF THE INPUT STAGE (STAGE 1)

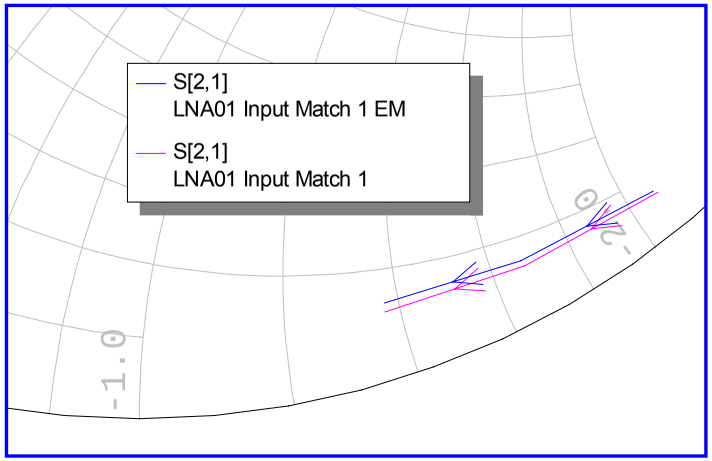
In order to try to reduce the difference between the simulation and the final result the input match circuit of the first stage of this LNA has been simulated because bending the long narrow line could produce some unpredictable effects. Using the AWR EM simulator, combined with the AWR Schematic, the results have been compared.

In the picture the Input Matching circuit of the stage1 without the bias network is showed. The investigation regarded what effect bending the line could be and if there should be some relevant interaction between the side of the narrow line and the edge of the larger one.



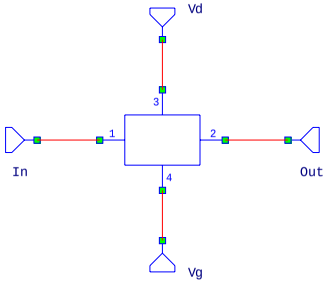
In the following graphics the simulations are showed. There is a difference between an EM simulation of a bent line and the circuital simulations of a straight line. This difference can be compensated by adding a 30um length line of the same kind of the narrow one.

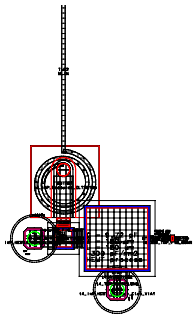


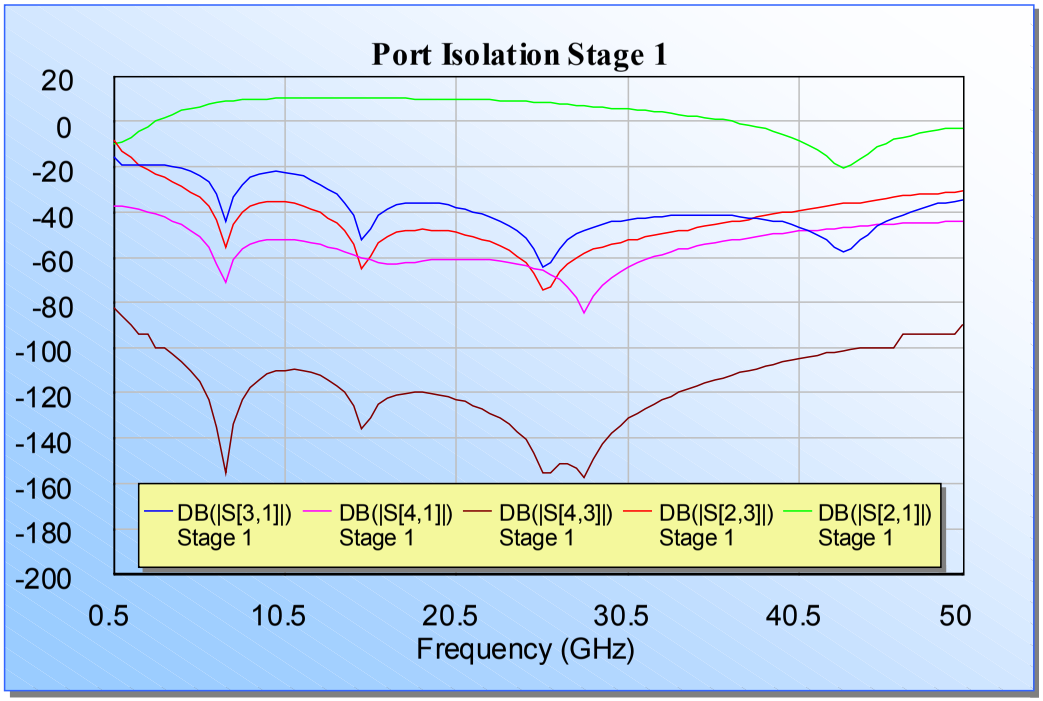


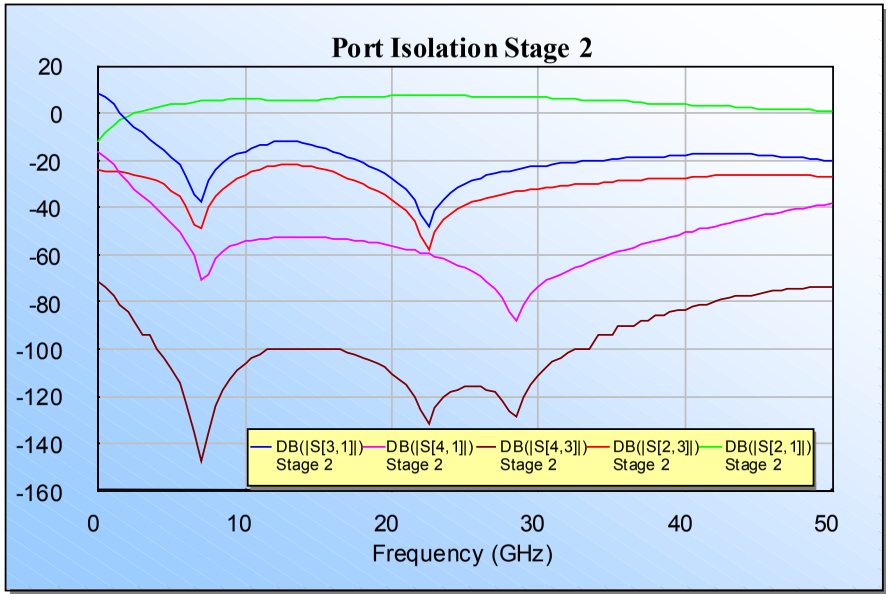
PORT ISOLATION

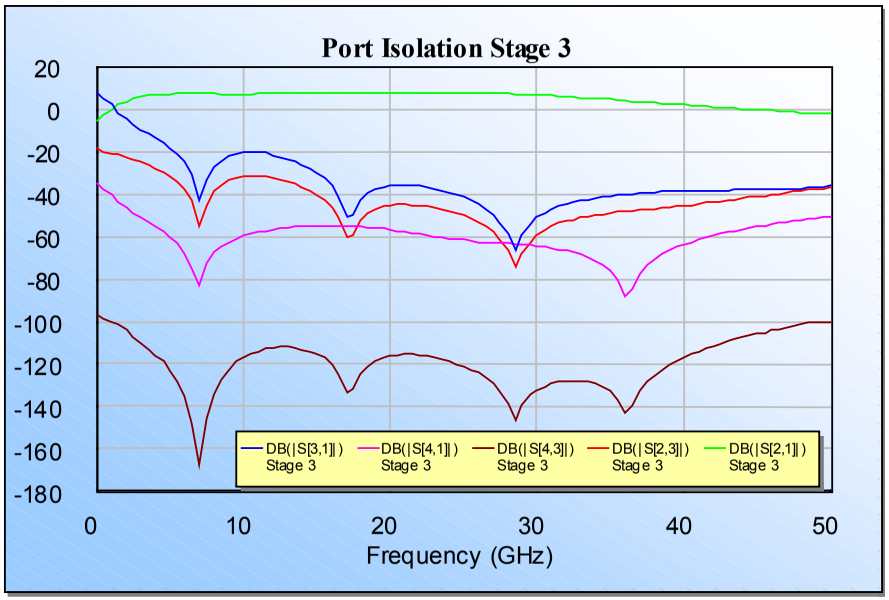
A single stage can be considered like a 4 port device. Ideally, the signal should be travelling from port 1 to port 2 while the 3 and 4 ports are connected to the biasing network and referred to ground. Practically, a small part of the signal could travel along the biasing network and if this is not properly filtered could cause oscillation. The isolation has been investigated and the results are indicated in the graphics.

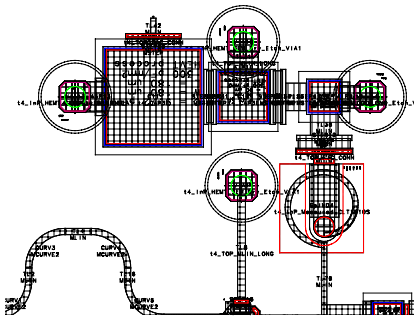


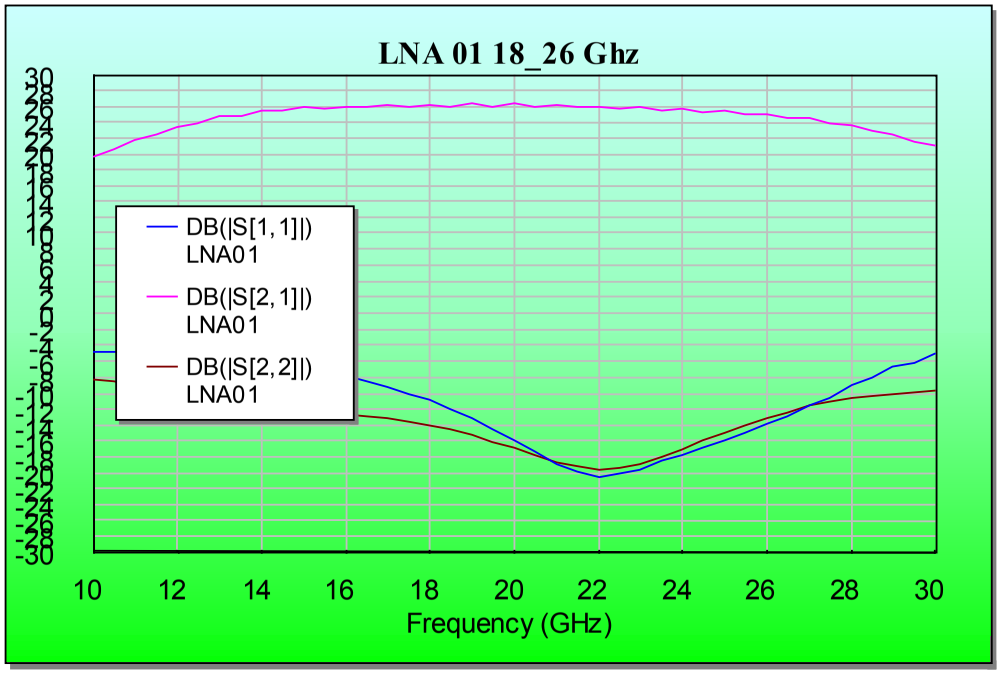


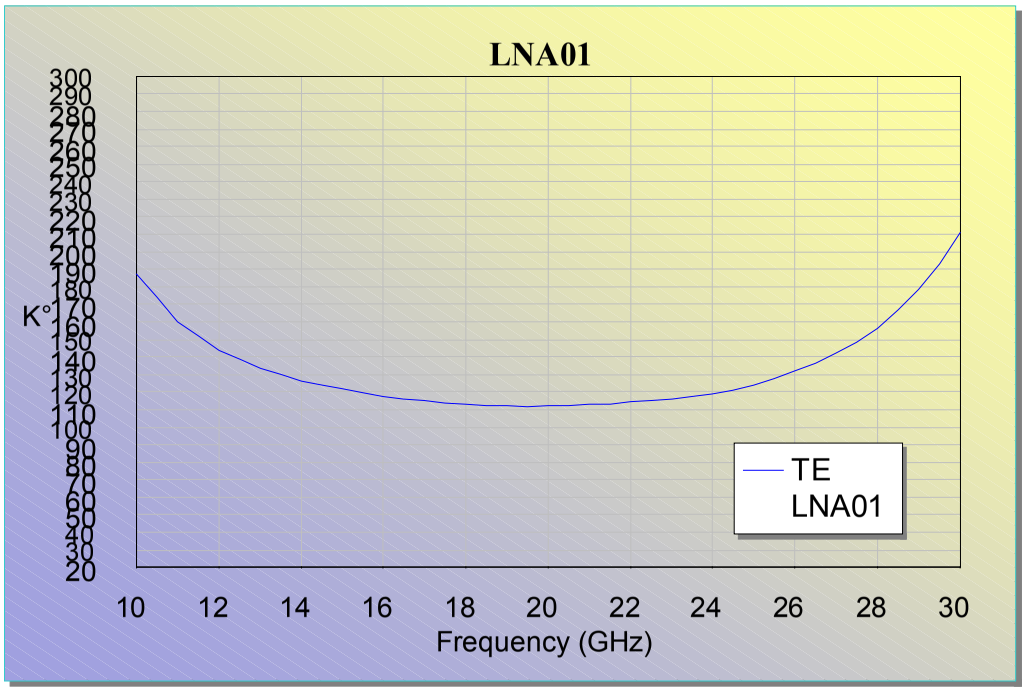


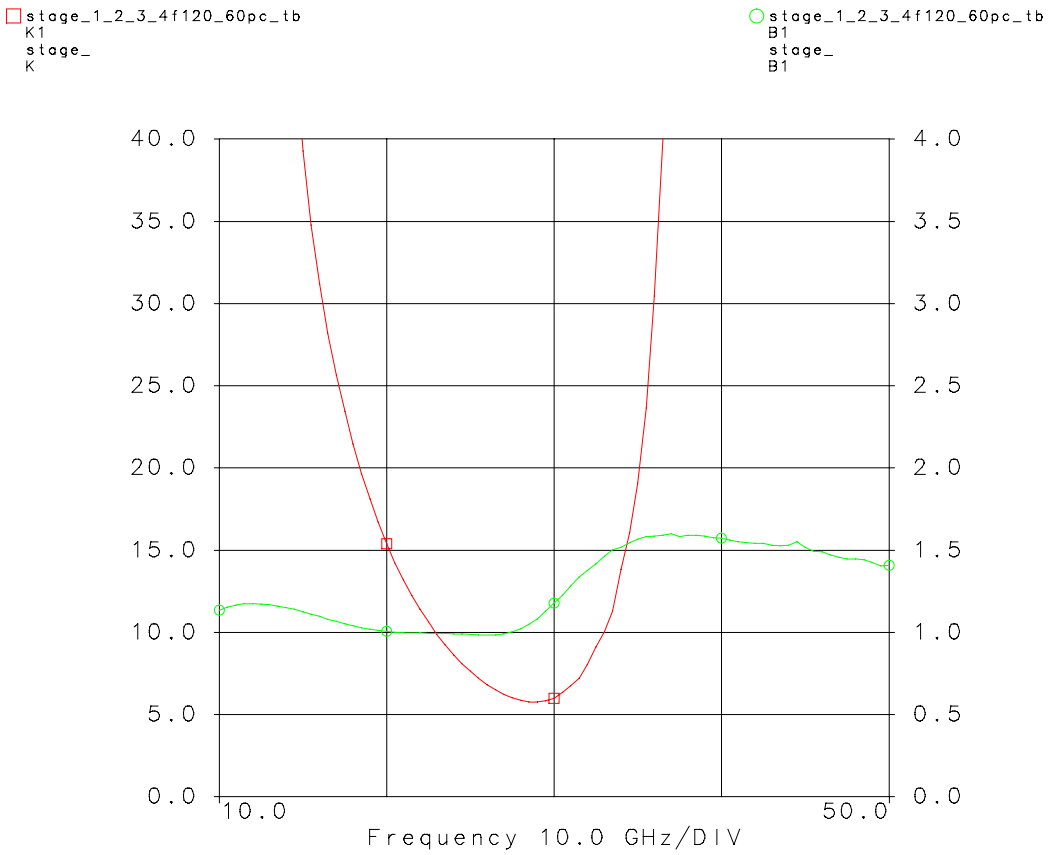

Port Isolation Stage 2
20
0
-20
-40
-60
-80
-100
-120
-140
-160
0
10
20
30
40
50
Frequency (GHz)
DB(|S[3,1]|) Stage 2
DB(|S[4,1]|) Stage 2
DB(|S[4,3]|) Stage 2
DB(|S[2,3]|) Stage 2
DB(|S[2,1]|) Stage 2

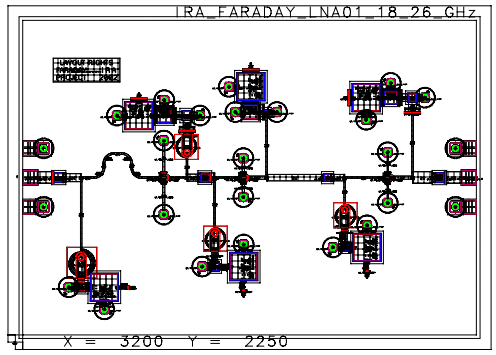

Port Isolation Stage 3
20
0
-20
-40
-60
-80
-100
-120
-140
-160
-180
0
10
20
30
40
50
Frequency (GHz)
DB(|S[3,1]|) Stage 3
DB(|S[4,1]|) Stage 3
DB(|S[4,3]|) Stage 3
DB(|S[2,3]|) Stage 3
DB(|S[2,1]|) Stage 3




LNA 01 18_26 Ghz
DB(|S[1,1]|)
LNA01
DB(|S[2,1]|)
LNA01
DB(|S[2,2]|)
LNA01
10
12
14
16
18
20
22
24
26
28
30
Frequency (GHz)


LNA01
K°
TE
LNA01
10
12
14
16
18
20
22
24
26
28
30
Frequency (GHz)


stage_1_2_3_4f120_60pc_tb
K1
stage_
K
stage_1_2_3_4f120_60pc_tb
B1
stage_
B1
40.0
35.0
30.0
25.0
20.0
15.0
10.0
5.0
0.0
4.0
3.5
3.0
2.5
2.0
1.5
1.0
0.5
0.0
10.0
50.0
Frequency 10.0 GHz/DIV

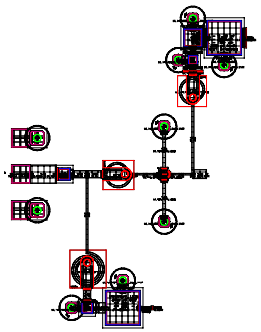

IRA_FARADAY_LNA01_18_26_GHz
X = 3200 Y = 2250

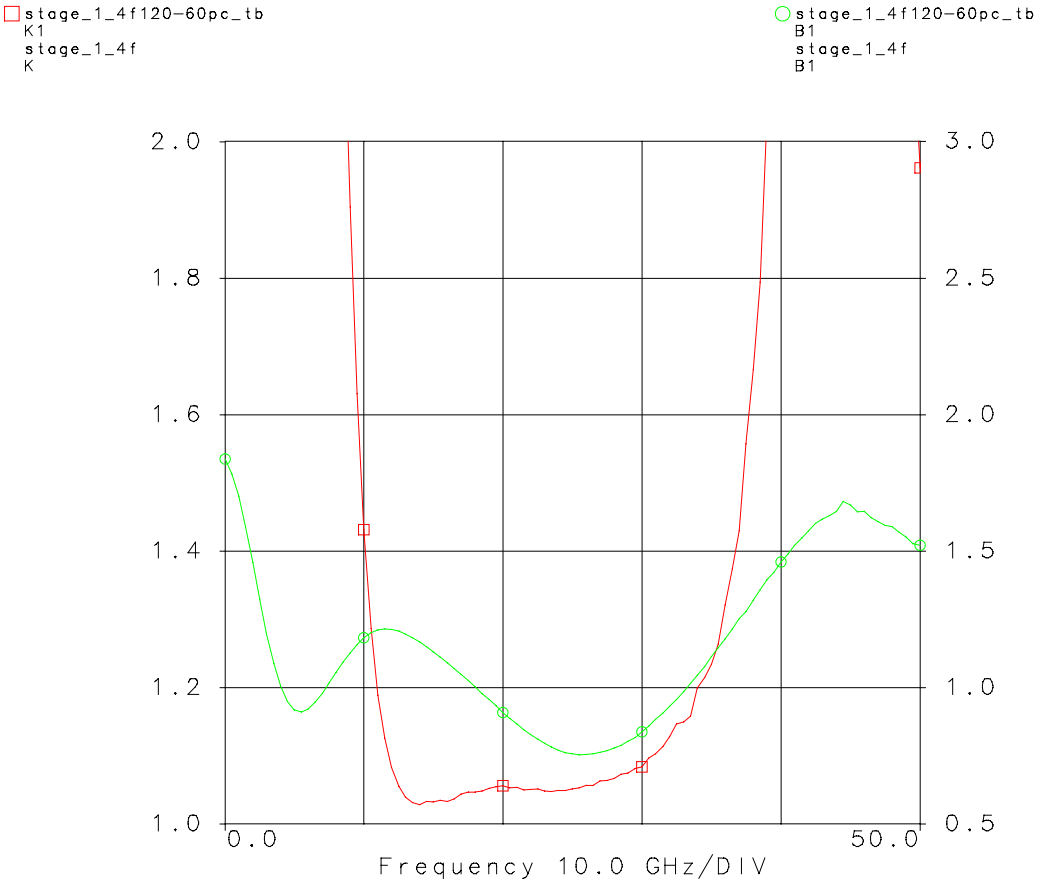
Low Noise Amplifier 18 to 26 Ghz Version 5 (November 11,2002)

Three stage 0.9 Vds 18 mA Idss

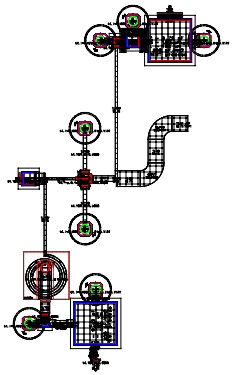
Stability stage description

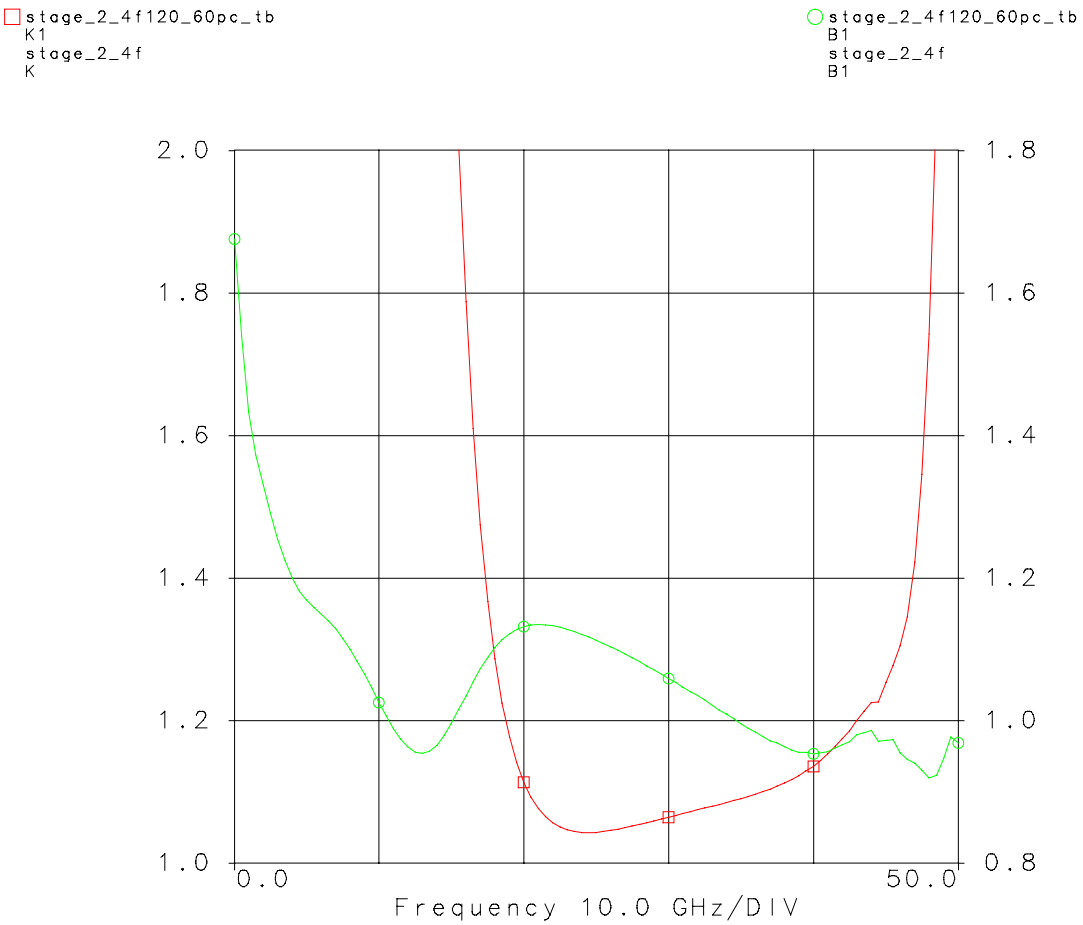
Stage 1



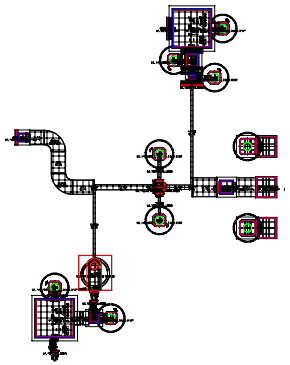


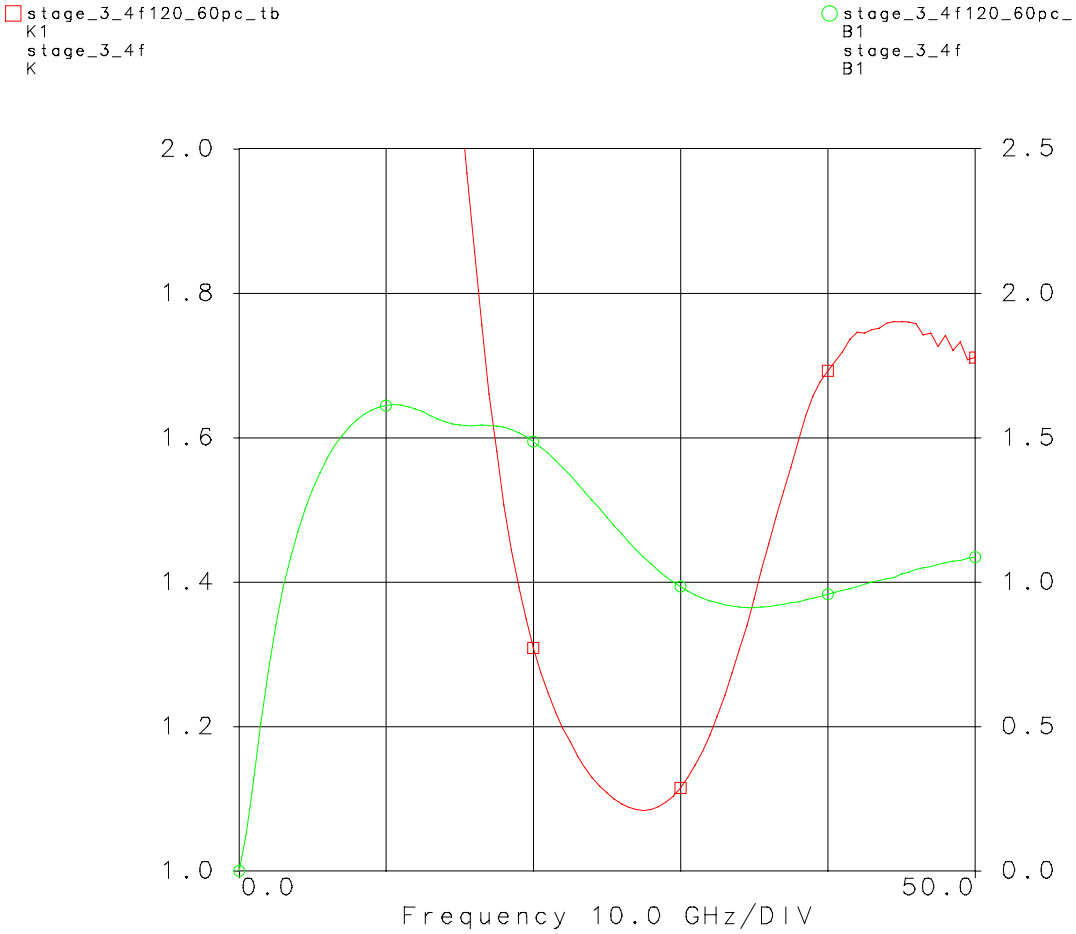
Stage 2




stage_2_4f120_60pc_tb
K1
stage_2_4f
K
stage_2_4f120_60pc_tb
B1
stage_2_4f
B1
2.0
1.8
1.6
1.4
1.2
1.0
1.8
1.6
1.4
1.2
1.0
0.8
0.0
50.0
Frequency 10.0 GHz/DIV

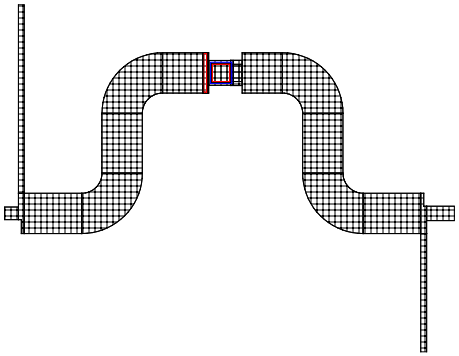
Stage 3



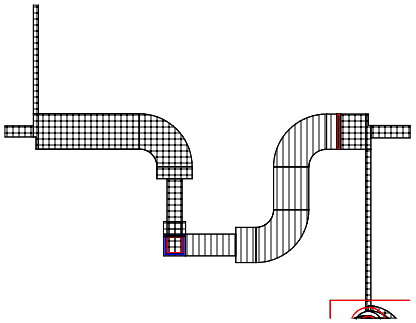

stage_3_4f120_60pc_tb
K1
stage_3_4f
K
stage_3_4f120_60pc_tb
B1
stage_3_4f
B1
2.0
1.8
1.6
1.4
1.2
1.0
2.5
2.0
1.5
1.0
0.5
0.0
0.0
50.0
Frequency 10.0 GHz/DIV

EM SIMULATION OF THE INTERSTAGE BETWEEN THE SECOND AND THE THIRD HEMT

In order to equalize the gain it was necessary to use a large and long microstrip line between the second and the third HEMT. The constraint against this necessity were the chip dimension. Two different solutions have been investigate and they are showed in the picture below. In the middle of the line there is a DC block capacitor:

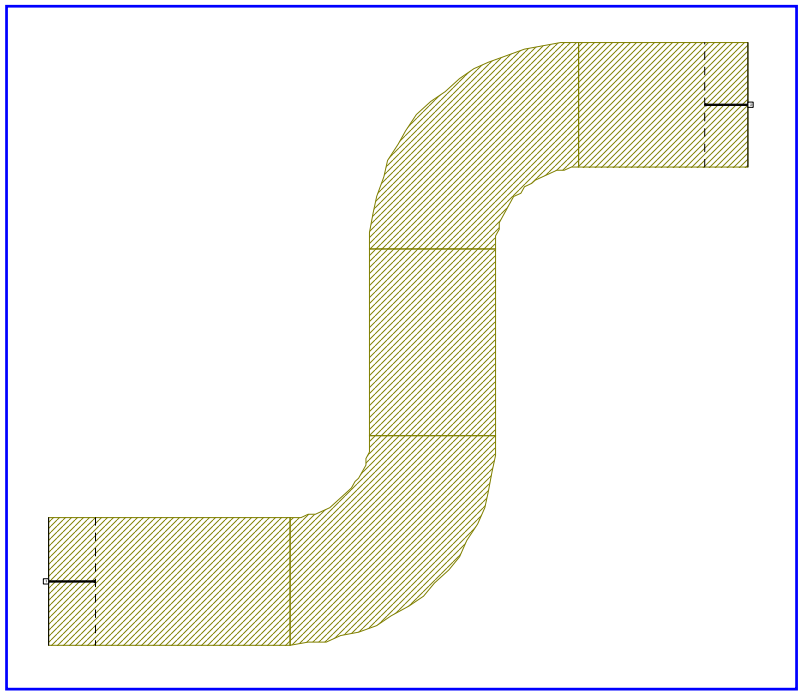


Solution A



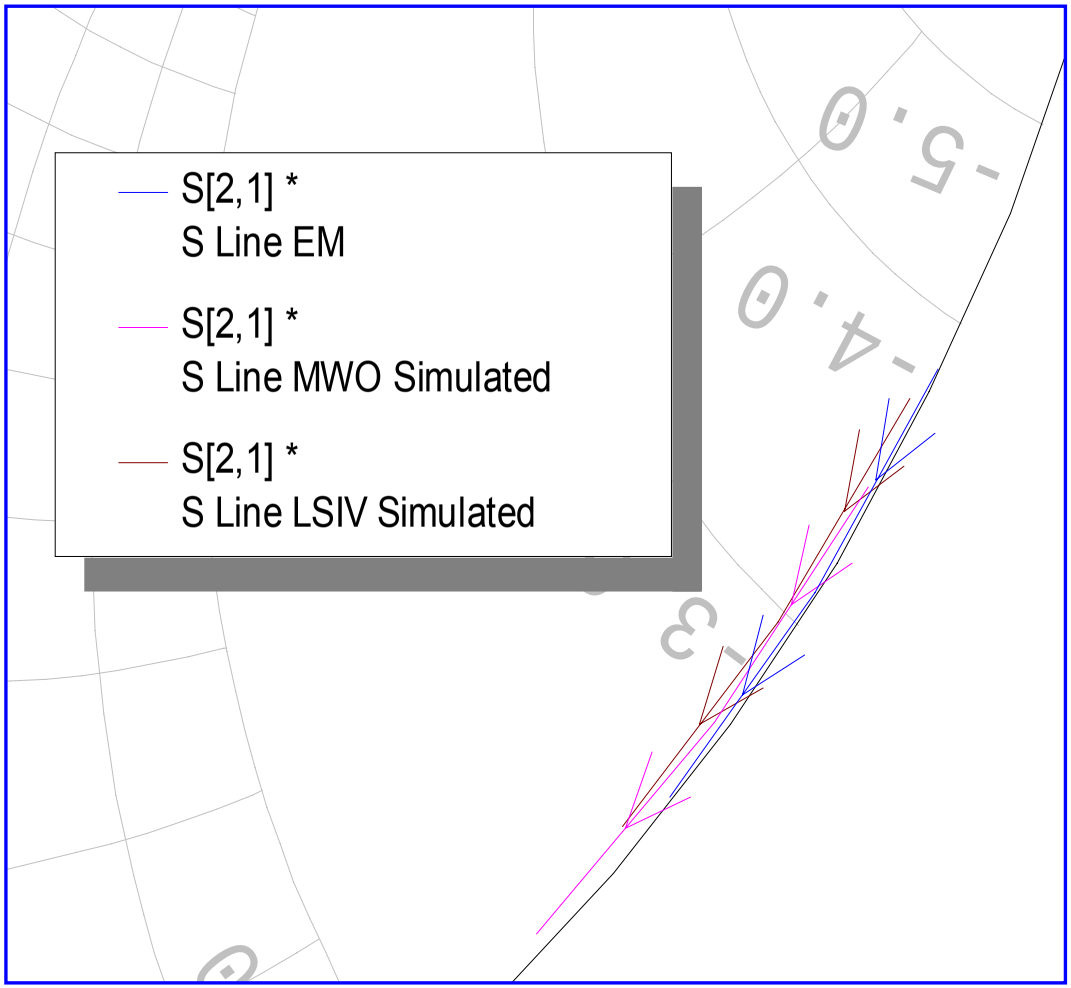
Solution B

The Solution A is less compact compared to solution B but appears less critical because A has less unpredictable electromagnetic behaviour than B. In the solution A the microstrip lines are both on the Top Metal layer and the distance from edge lines is at least two times the substrate thickness. The bend radius is wide enough to minimize the EM effects due to bending. In the solution B the capacitor ports are 90° placed. The right part of the line is on the FIC (bottom) metal layer and it is connected again to the top metal layer after the second bend using FIC to TOP via's. In order to avoid line edge coupling we must use some pieces of narrow line, but this modification changes the network response. In order to reduce the difference between simulation and the final result due to unpredictable electromagnetic effects, the S line has been simulated using the AWR EM simulator combined with the AWR Schematic. The AWR results and the curve model of LIBRA Series IV have been compared.



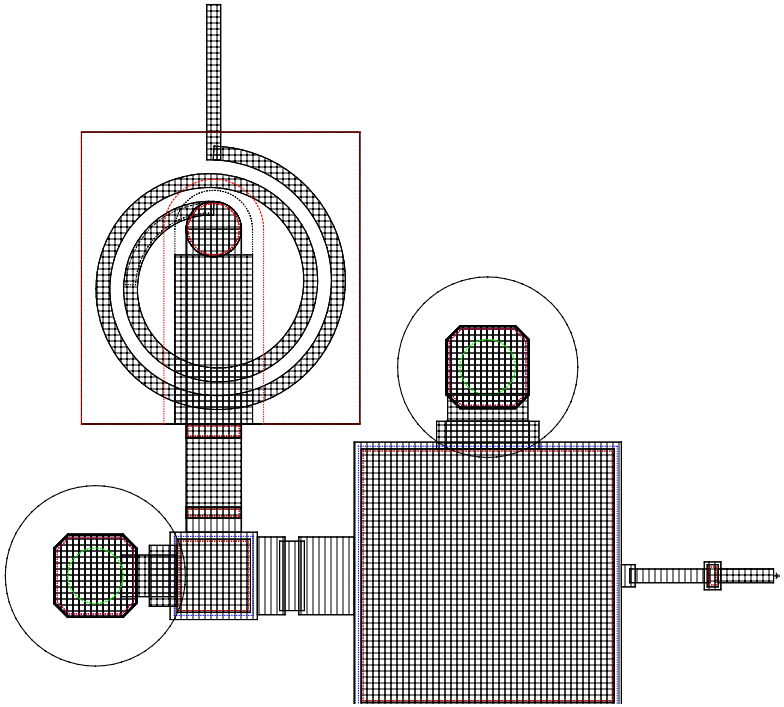
There are some differences between an EM simulation and the circuital simulations of a bent line. The Libra Series IV curve model is better than MWO2001 curve model and the differences of the EM simulation are not so relevant and have no relevant effects on the LNA performances. In the graphic the results are showed.

In the picture the line under test is represented. It has been investigated what kind of effect could have bending the line and if there could be some relevant interaction between the line sides.

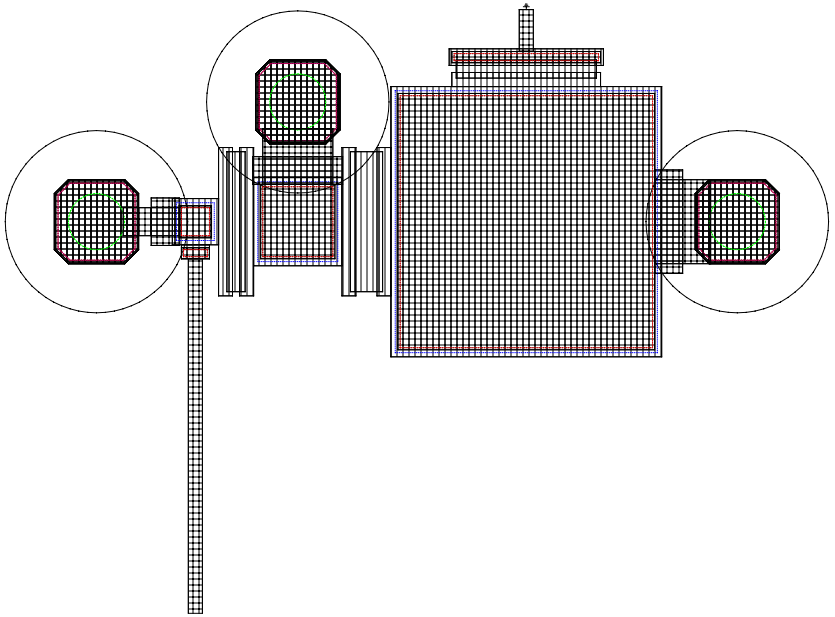


PORT ISOLATION

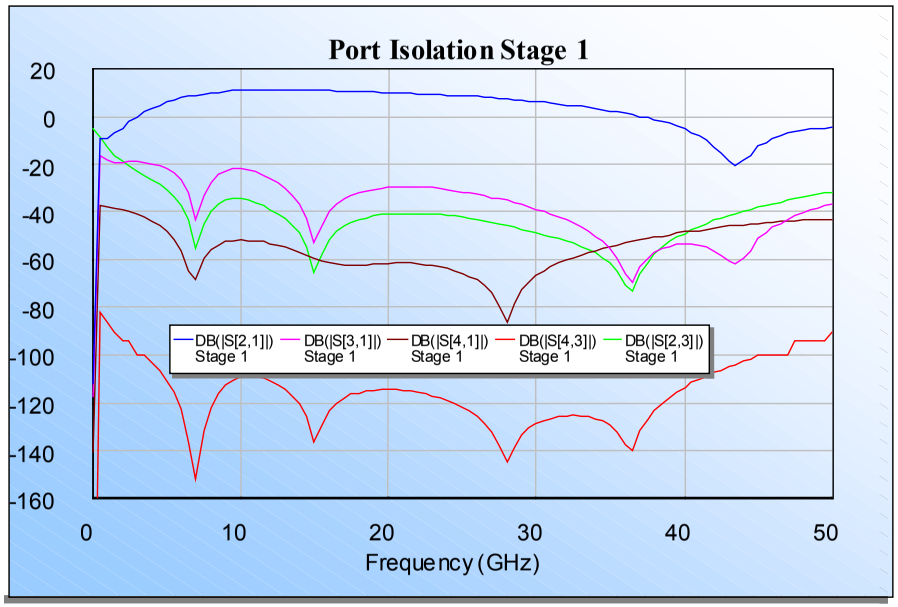
A single stage can be considered like a 4 port device. Ideally, the signal should be travel from port 1 to port 2 and the 3 and 4 port are connected to the biasing network and referred to ground. Practically, a small part of the signal could travel along the biasing network and if this is not properly filtered could cause oscillation. The isolation has been investigated and the results are indicated in the graphics on the next page. In this page some bias network samples are represented.

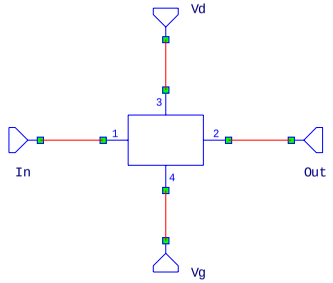


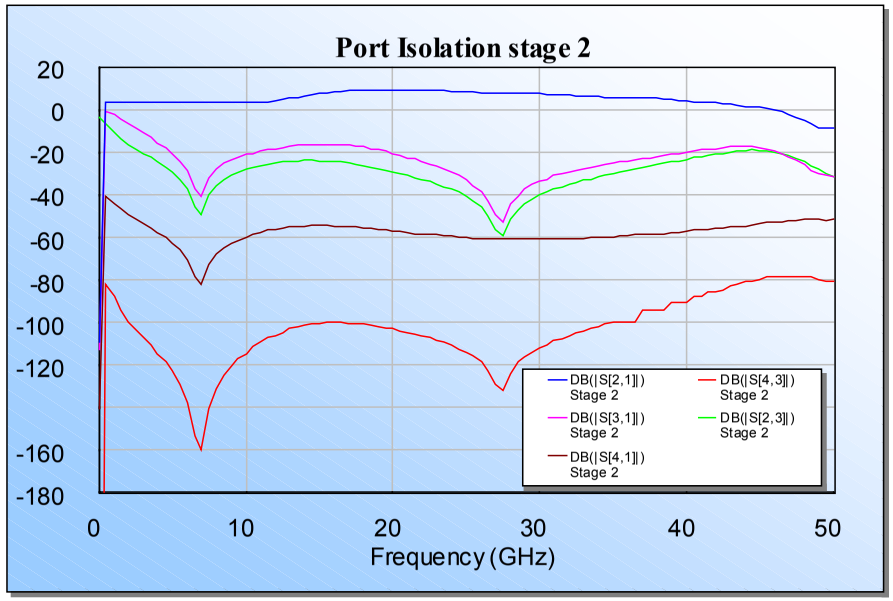
Gate bias network Stage 1

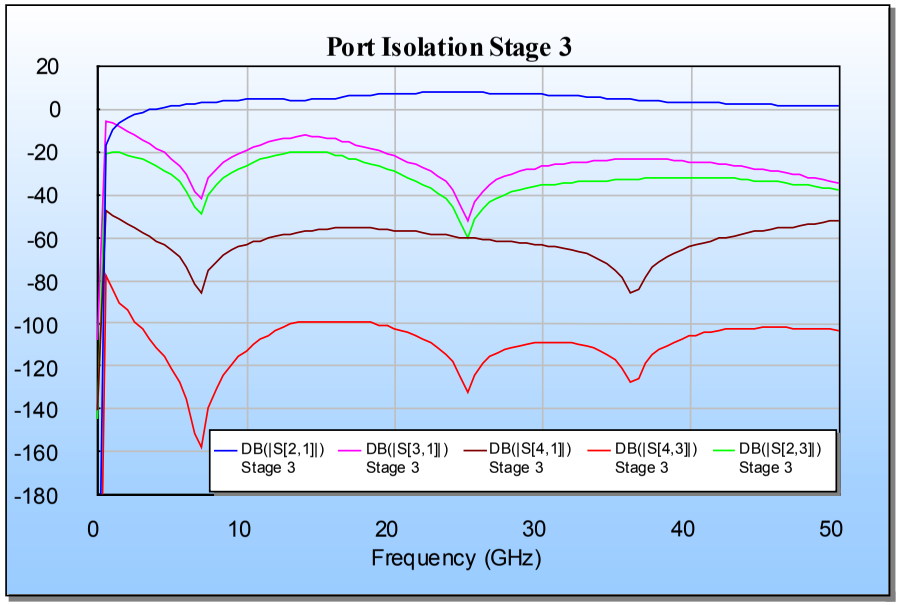


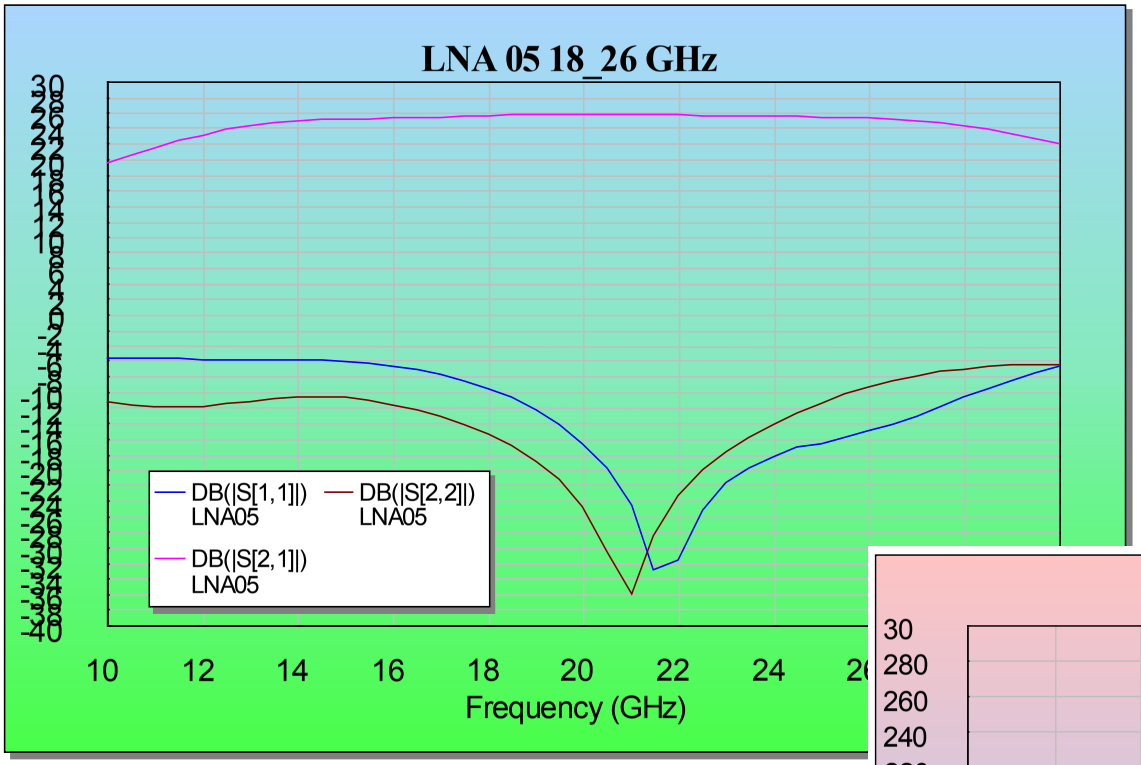
Drain bias network Stage 2


Port Isolation Stage 1
20
0
-20
-40
-60
-80
-100
-120
-140
-160
0
10
20
30
40
50
Frequency (GHz)
DB(|S[2,1]|) Stage 1
DB(|S[3,1]|) Stage 1
DB(|S[4,1]|) Stage 1
DB(|S[4,3]|) Stage 1
DB(|S[2,3]|) Stage 1


Vd
3
In
1
2
Out
4
Vg

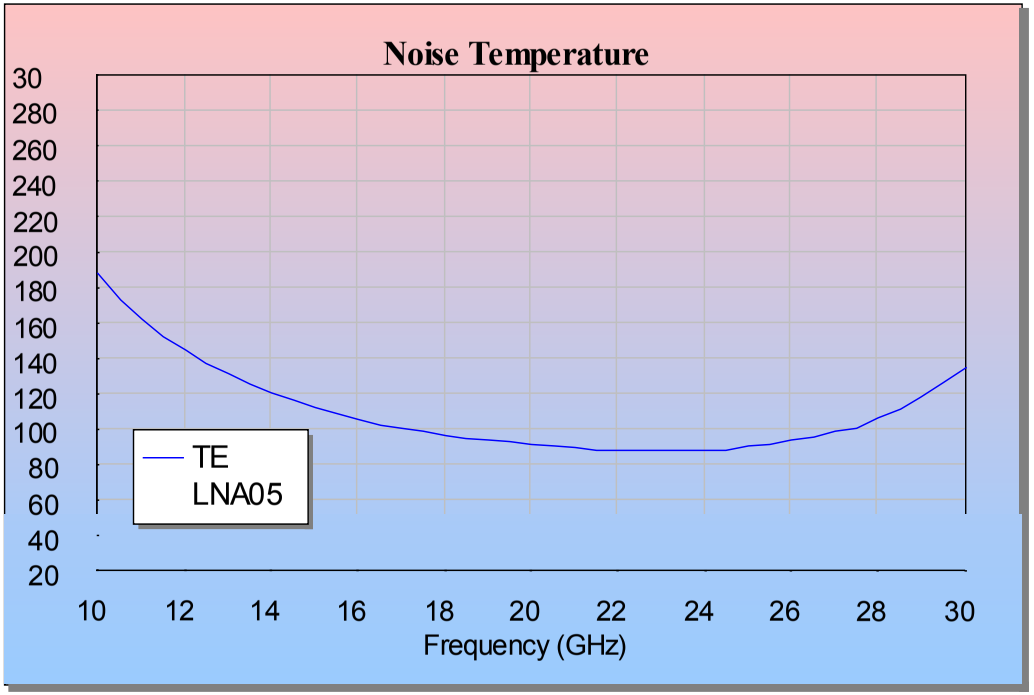

Port Isolation stage 2
20
0
-20
-40
-60
-80
-100
-120
-160
-180
0
10
20
30
40
50
Frequency (GHz)
DB(|S[2,1]|) Stage 2
DB(|S[3,1]|) Stage 2
DB(|S[4,1]|) Stage 2
DB(|S[4,3]|) Stage 2
DB(|S[2,3]|) Stage 2


Port Isolation Stage 3
20
0
-20
-40
-60
-80
-100
-120
-140
-160
-180
0
10
20
30
40
50
Frequency (GHz)
DB(|S[2,1]|) Stage 3
DB(|S[3,1]|) Stage 3
DB(|S[4,1]|) Stage 3
DB(|S[4,3]|) Stage 3
DB(|S[2,3]|) Stage 3

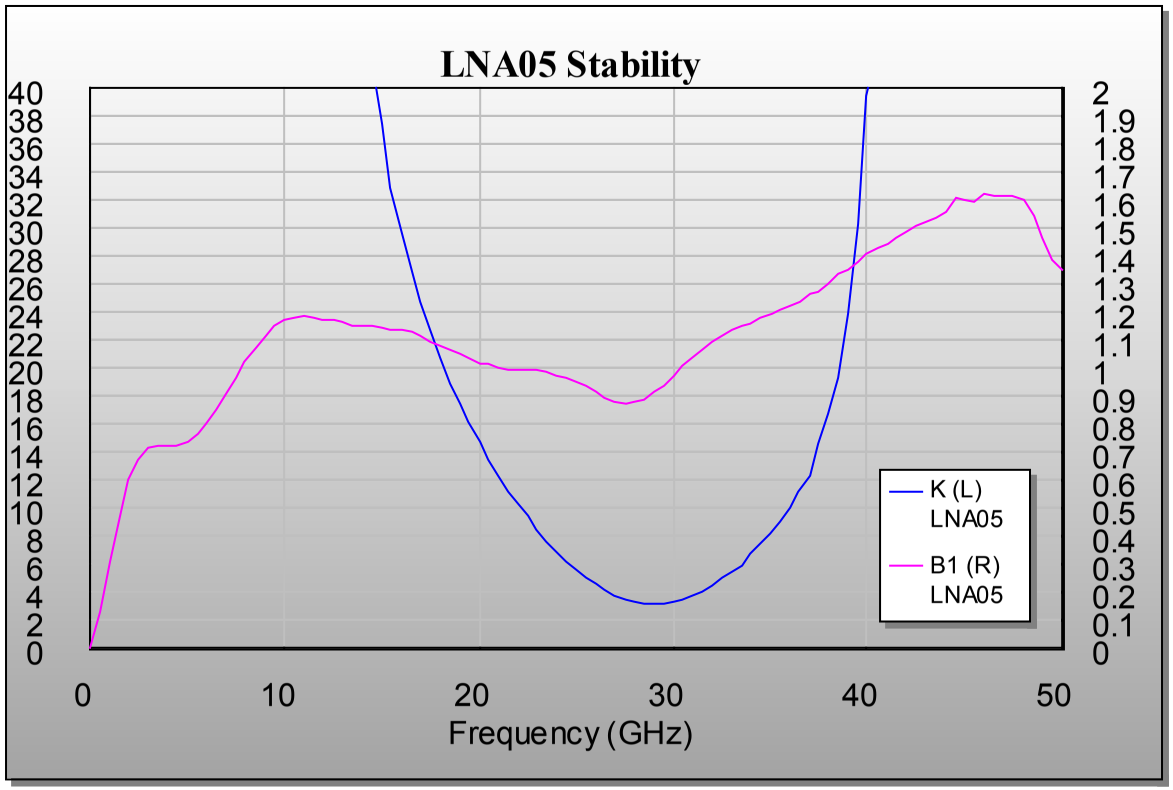


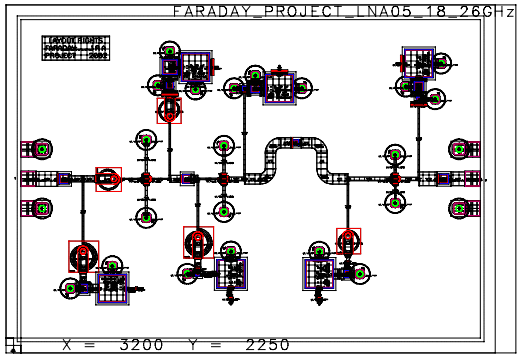
		S Parameters [dB]		
		S11	S21	S22
Frequency [GHz]	18	-9.49	25.6	-11.7
	22	-31.7	25.6	-23.4
	26	-15.3	25.3	-9.39

	Te @ 300 [K°]
Frequency [GHz] 18	96.8
22	88.6
26	93.8



STABILITY OF THE COMPLETE LNA05





The design of LNA2 follows similar layout of the LNA1 but needs only two stages to achieve the desired gain.

2. FEED HORN, PASSIVE COMPONENTS AND DEWAR

In the present phase the IRA-Florence section is working on the design and construction of the front-end passive components (horn and polarizer) and of the dewar for the receiver array.
In the following a review on the status of the project is given.

2.1 Dual profiled corrugated feed horn

Feed design is performed on the basis of mode matching techniques according to the following parameters which account for the optical Cassegrain configuration of Medicina and Noto VLBI radiotelescopes:

- Center frequency 22 GHz
- Bandwidth >20%
- Edge taper 12 dB at 9.5^0
- Crosspolarization < -25 dB
- First sidelobes < -30 dB

The feed has been designed according to dual profiled shape geometry as shown in fig. 2.1.1. In the same figure the phase center position computed for an edge taper of 12 dB is indicated.

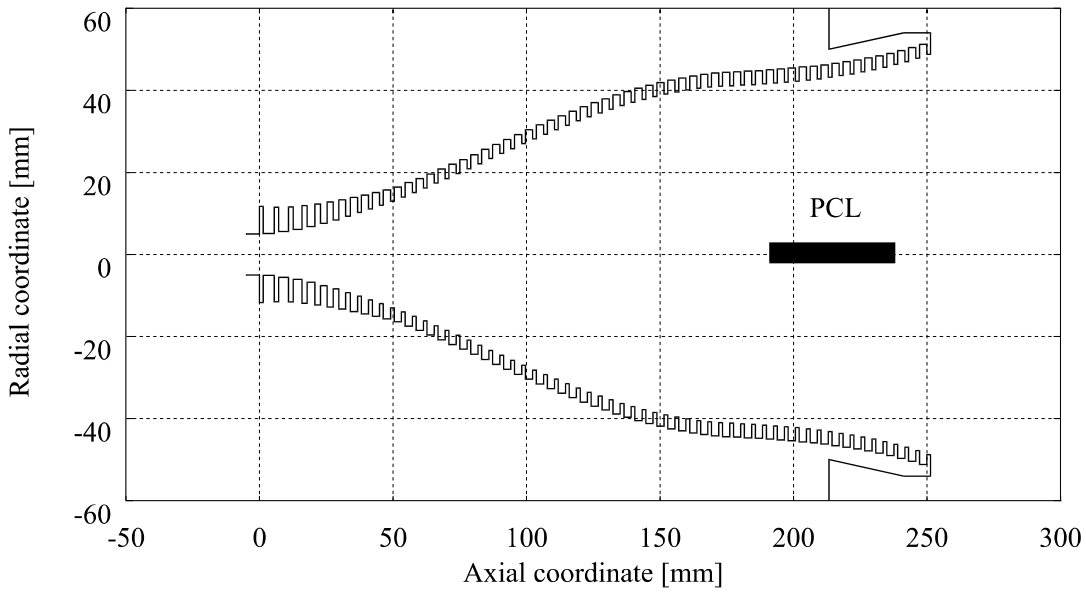


Fig. 2.1.1 Horn geometry

The return loss and crosspolarization of the feed is shown in fig. 2.1.2

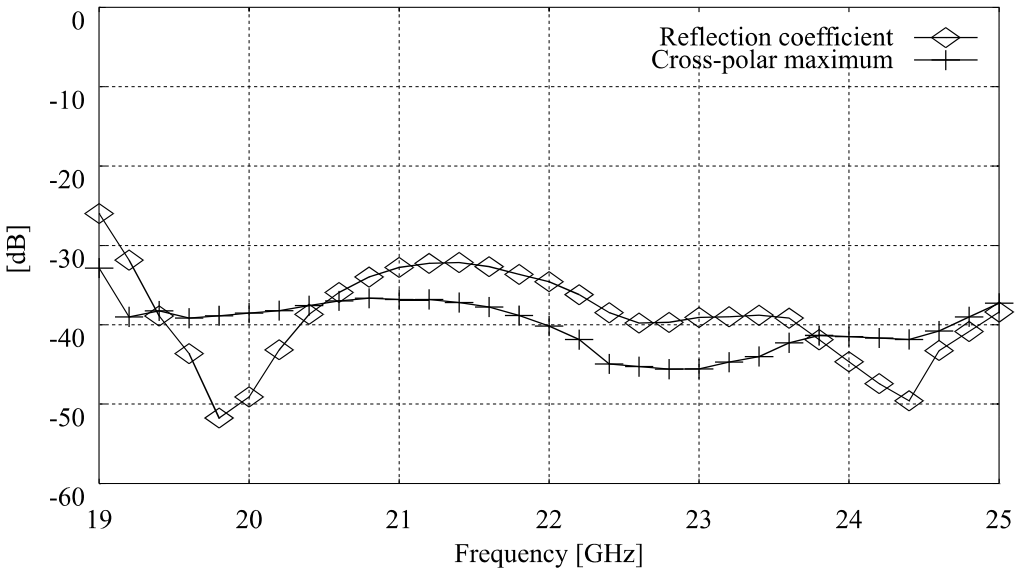


Fig. 2.1.2 Horn computed parameters

The beam patterns for the E plane, H plane and 45 deg. plane are shown at 19, 22 and 25GHz respectively in the figuree 2.1.3a, 4a and 5a. The phases are reported in the figures 2.1.3b, 4b and 5b.

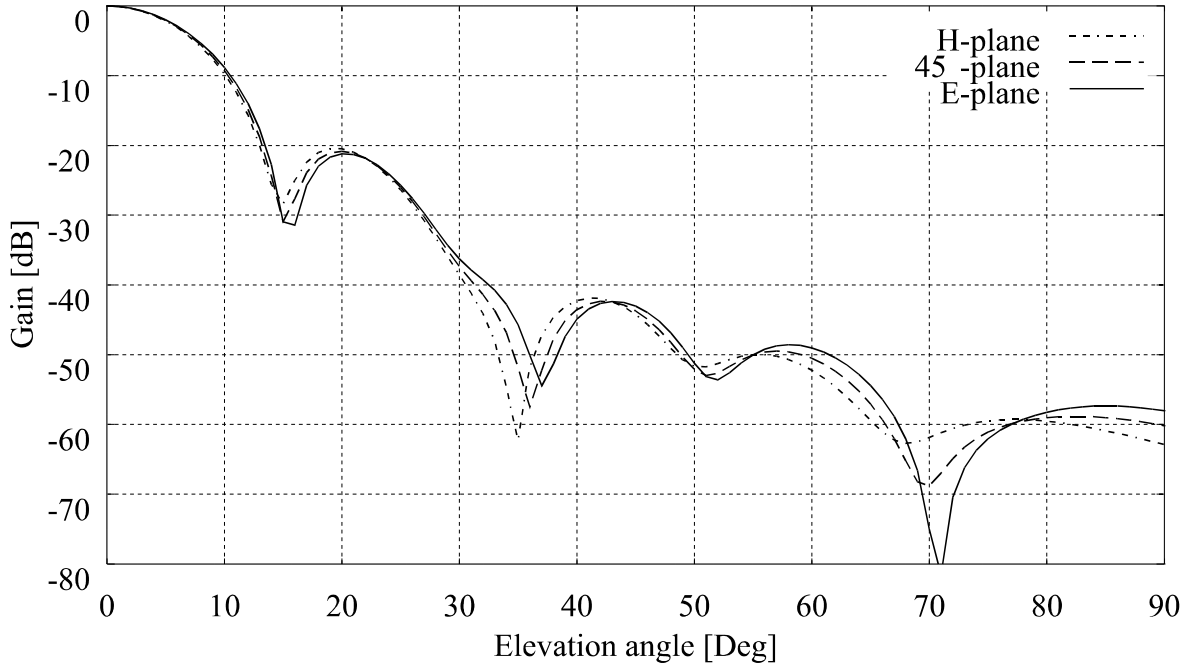


Fig. 2.1.3a Beam pattern at 19 GHz

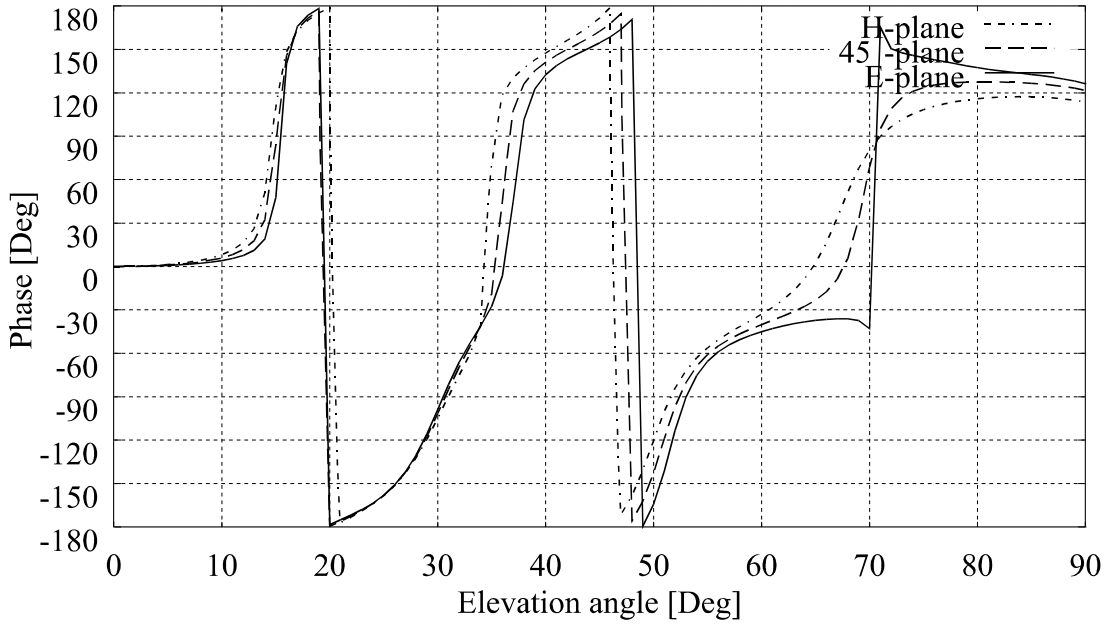


Fig. 2.1.3b Phase pattern at 19 GHz

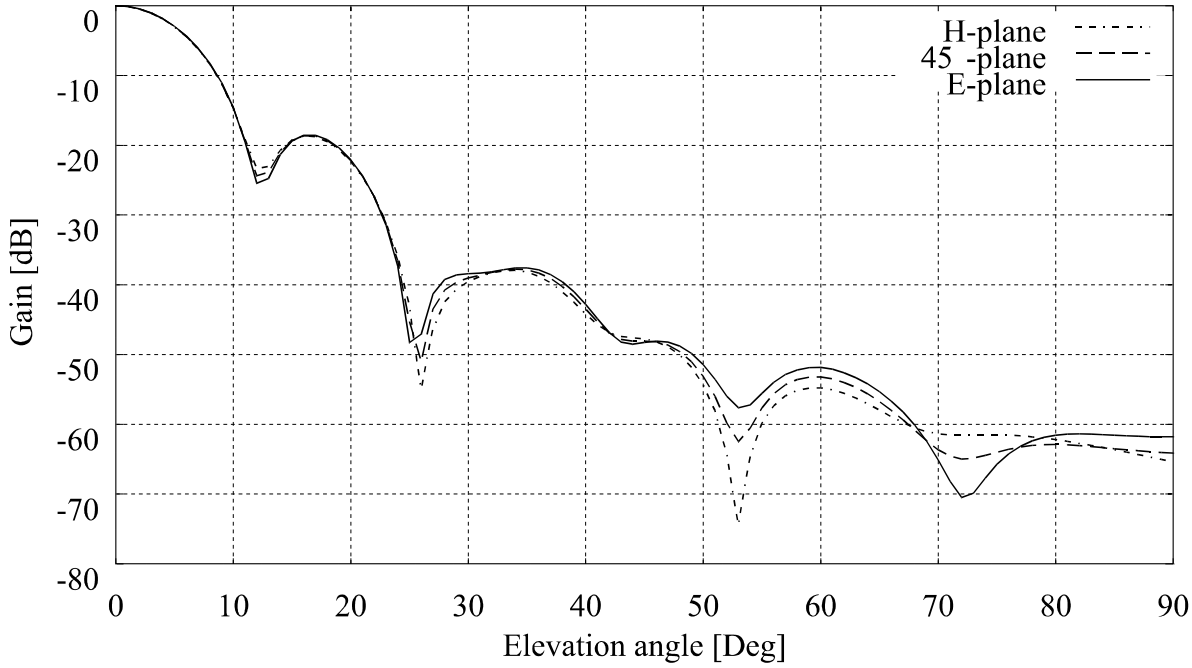


Fig. 2.1.4a Beam pattern at 22 GHz

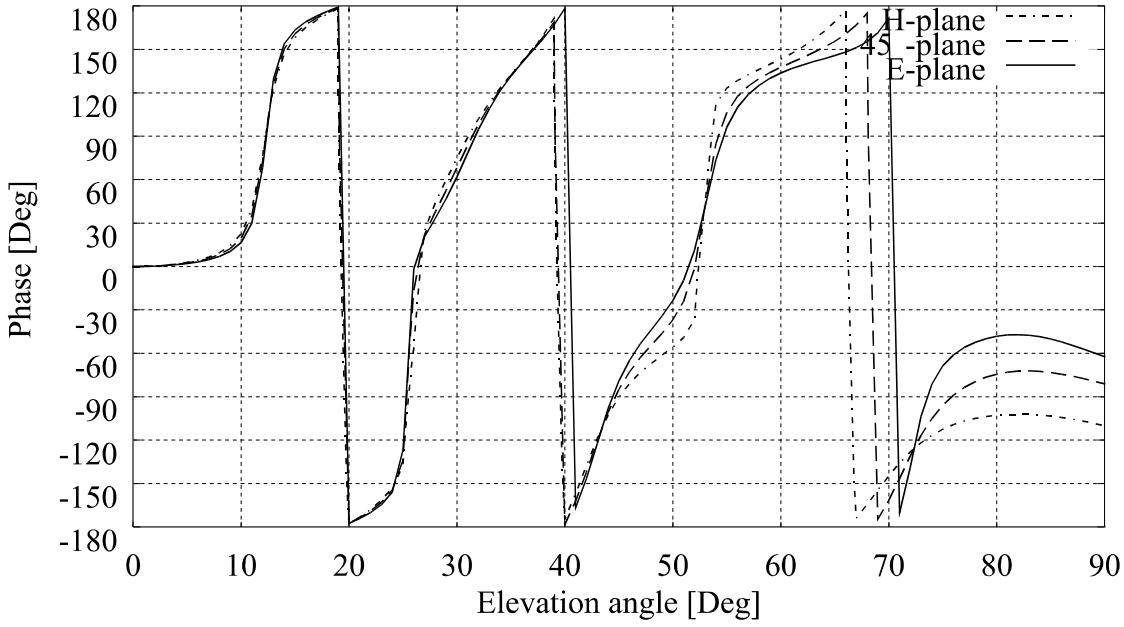


Fig. 2.1.4b Phase pattern at 22 GHz

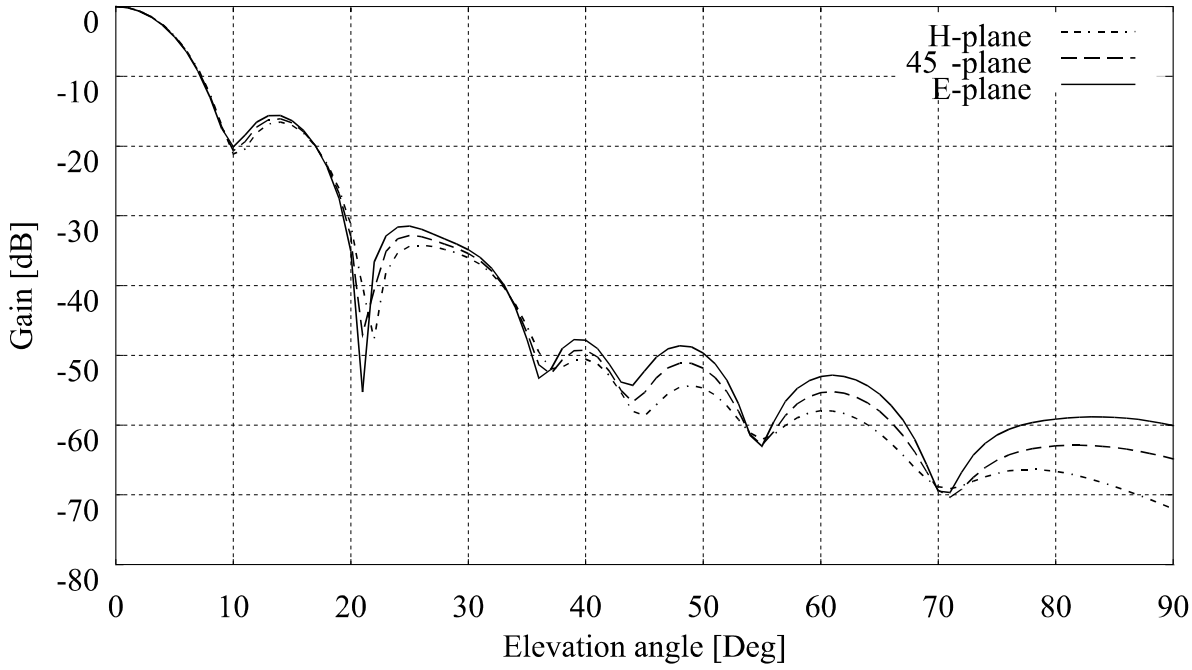


Fig. 2.1.5a Beam pattern at 25 GHz

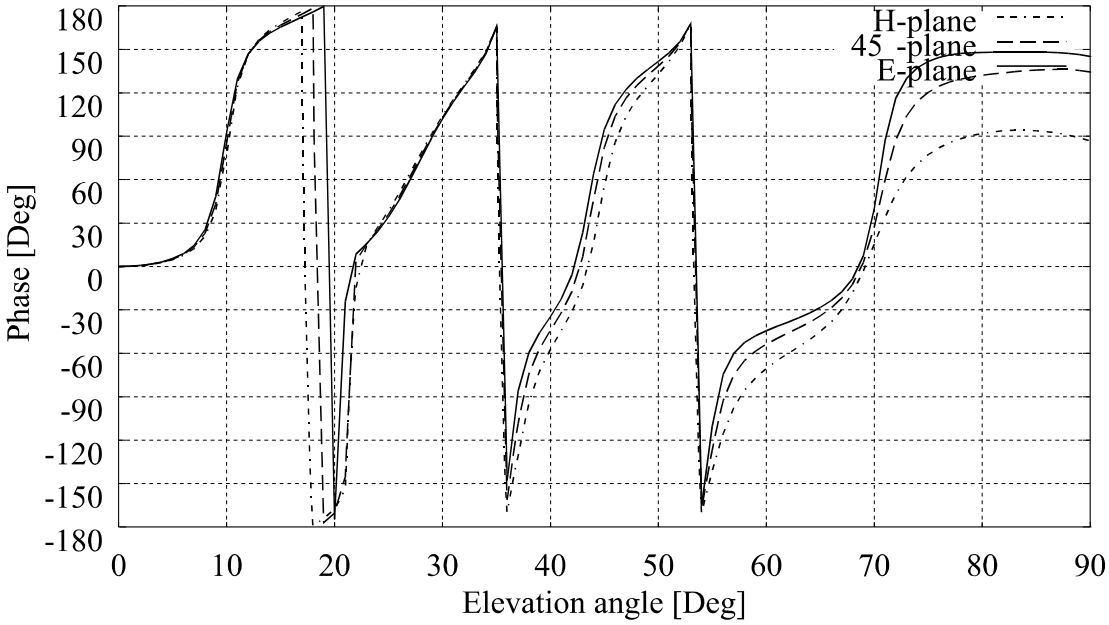
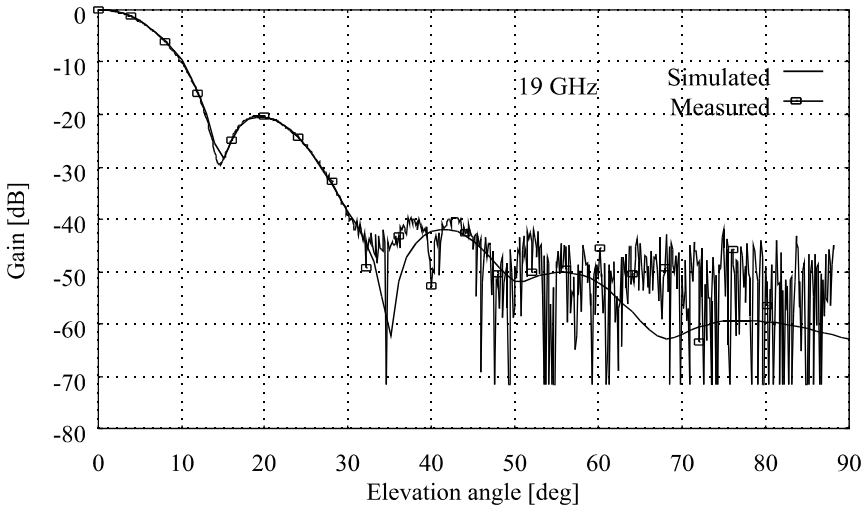


Fig. 2.1.5b Phase pattern at 25 GHz

Anechoic room measurements of the beam patterns at 19 GHz (upper panel), 22 GHz (middle panel) and 25 GHz (lower panel) are reported in fig. 2.1.6.
One can observe the excellent agreement between the computed and measured value of the beam pattern. A picture of one out of five horn is shown in Fig. 2.1.7.



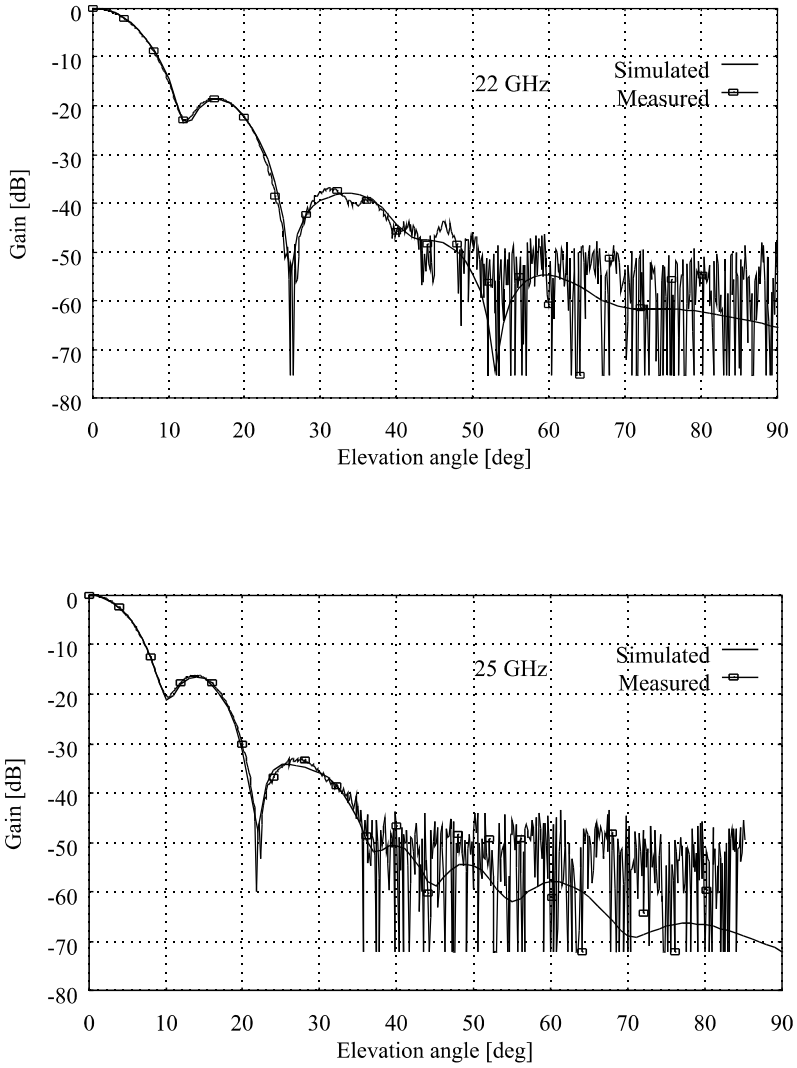


Fig. 6: Feed horn beam pattern measurements at 19 GHz (upper panel) 22 GHz (middle panel) and 25 GHz (lower panel)

Fig. 2.1.7 . Photo of the corrugated horn for the array receiver.

2.2 Polarizer and OMT

Both the polarizer and OMT are still in preliminary design phase.

2.3 Dewar

Horn geometrical size and the array configuration define the overall structure of the dewar. The geometry of the 5 receivers array is shown in fig. 2.3.1 and a picture is in fig. 2.3.2.
A prototype dewar has been manufactured and tested with the five feed horns installed. The CTI 350 was used as cryogenerator. The mechanical structure supporting the horns is cooled down by means of 4 thermal straps, each made by 4 copper foils 25 mm large, 0.5 mm thick. The vacuum window is made by 50 μm thick mylar. Thermal filters are a sheet of black poly 0.05 mm thick on the thermal shield at 70K plus a piece of PP2 (Eccosorb) 6 mm thick at 300 K.

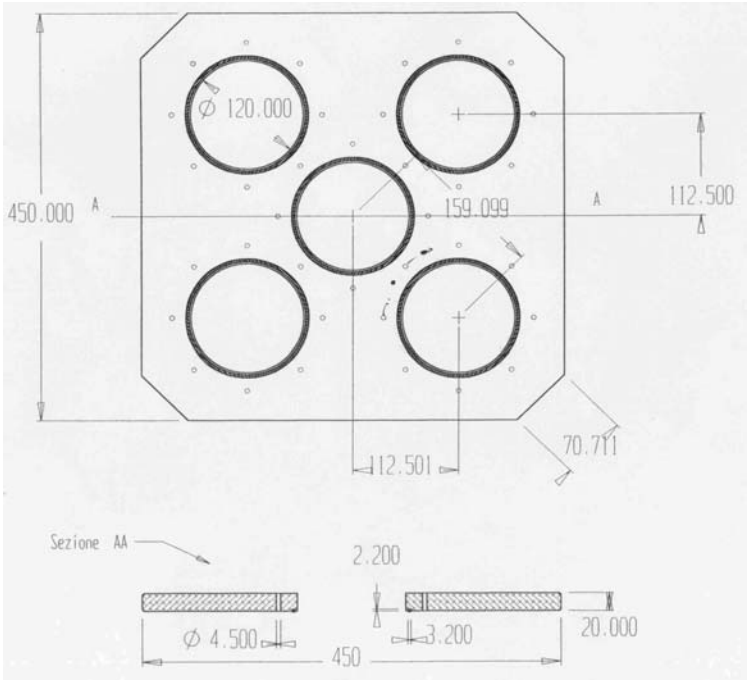


Fig. 2.3.1 Array geometry

The measured performances are:

- Cooling time to reach a temperature < 20 K on the cold finger : 35 hours
- Horn temperature near the output waveguide : 18 K
- Horn temperature at aperture : 25 K
- No wet windows

Fig. 2.3.2 Feed horns installed into the dewar.

3. WAFER ANALYSIS

The evaluation about the wafer capability has been based on the available information.

- Wafer diameter is 3 inches (76.2 mm) (Fig. 3.1)
- Each foundry run produces 6 identical wafers (obtained by the same mask)

From each run we may expect at least 3 successful wafers (it is possible that process and quality of wafers may be improved meanwhile).
Now looking at fig. 3.1, where **A** is a typical round wafer, the area is divided into identical cells, each one representing a frame **C**. The wafer area is about 4600 mm^2 and the inner square **(B)** is 2900 mm^2.
The effective area is in between the two figures as:

- Some of the frames are limited by the circular geometry and the inside circuits are no longer usable,
- Near wafer edges circuits within frames tend to exhibit more defects and are better skipped (this is usually a trend, which may not be the case for TRW)

From these assumptions we may realistically evaluate an useful area of 3500 mm^2.

About frames, also exploiting information from R. Gough (CSIRO), two configurations are possible: a first one has only one type of frame (as in fig. 3.1), in a second configuration two types of frames are possible (probably alternate).
In any case the second hypothesis is always done because the foundry will need to insert ad-hoc circuits (PCM) for the process control.
However assuming the most of frames are of the same size, we may consider frames of 7.5x19.3 mm (about 150 mm^2) done by Gough. If so, each wafer could be split into 3500/150 = 23 frames. We approximate this figure to 20 owing to the need of the foundry to put their own PCM.
Into each frame we have the chips (numbers in **C**). They can be equal or different in size as first and last row in **C**. It is important that the frame can be cut along a straight line. Then circuits must have some common sizes and for this reason we will be asked to define individual chip sizes in order to design the frame. The dimension of the 22GHz chips are reported in section 1 of this report.
Of course the number of circuits will depend on their sizes. A three stages LNA fills 7 mm^2 . With this typical size we may expect within a frame 150/7 = 20 chips.
In summary the total number of circuits with different typology in a run (assuming different chips in a frame) is included between 20 frames x 3 wafer = 60 (3 wafers delivered) and 20 x 6 = 120 (6 wafers "good"). Total chip number will be included between 60 chip/type x 20 types = 1200 chips and 120 chip/type x 20 types = 2400 chips.
According to Gough, the yield may account for an efficiency between 40 and 90%. These are not usable numbers, as they rely on many parameters such as chip sizes, active elements in the chip, etc. We may tentatively state a figure of 50% for successful chips, thus limiting the number of chips between 600 and 1200 in the two hypothesis.
Each of the three partners will have 1/3 of these figures (200-400).

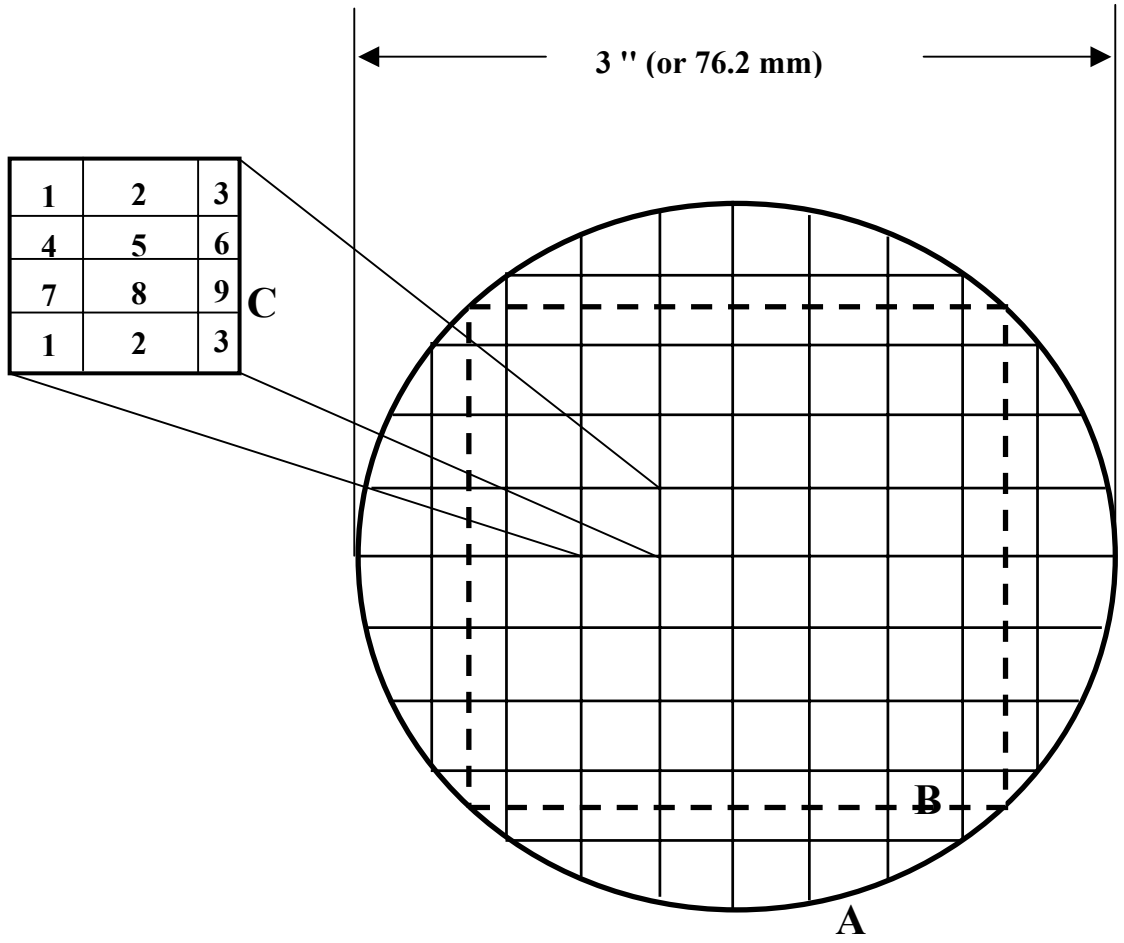


Fig. 3.1 Schematic of a wafer

4. MIXER

A preliminary approach to the mixer design refers to specifications of commercially available devices [5,6], as following:

RF bandpass 18-26 GHz
IF bandpass 7.9-8.9 GHz
Conversion loss 7 dB
Noise figure 8 dB
LO power 7-10 dBm
IP3 15 dBm
LO/RF port isolation 25 dB

There are some examples of InP solutions for such down converters, with the aim of integration with LNA devices [3,4].
Such mixer may work at ambient temperature thus avoiding the issue of the cryogenic temperature which may also vary the frequency response of the device [7].
At the beginning of the Faraday project IRA partner would try to design a dedicated mixer for the receivers. Due to the impossibility of the Jodrell Bank partner to support a 22GHz LNA design we deviated the work on the design of these last devices, crucial for the subproject 2, and decided to buy commercial mixers.
The choice was the MITEQ component AR1826L15G, an active mixer with the following characteristics

- RF bandpass 18-26 GHz
- IF bandpass 7.9-8.9 GHz
- Conversion gain 23 dB
- Noise figure < 3.5 dB
- LO power -3 dBm
- LO/RF port isolation < -48 dB

5. IF SIGNALS ROUTING

The array system provides 10 IF channels, five coming from left circular polarization and five from right polarization. These signals must be routed to the back end located in the antenna control room, about 100m away from the array location. The way for sending these signals must be carefully examined, because it implies a great amount of bandwidth routed. This is particularly true in view of larger arrays at higher frequencies (for example in the frame of the feasibility study of a 50-horn array at 50GHz): a huge amount of channels and bandwidth will be involved.
The trivial solution to add one more coaxial cable per channel could be a way in the case of ten channels but it is not for 100 channels!
But also the trivial solution for the 22GHz array probably is not feasible: the receivers have to be integrated in the already existing observing system of the antenna and constraints such that space available in the cable wrap are a concern. In any case a survey of possible solutions call for:

1. one coaxial cable per channel
2. frequency division multiplexing of channels
3. using one fiber optic cable with many fibers inside

Best frequency performance coaxial cables are 16mm in diameter, at least, but they are usable on the antenna truss. Inside the cable wrap a different cable, more flexible, has to be used so connections have to be provided. Fiber optic cable with twelve fibers inside is 8.2mm in diameter, it can be used also in the cable wrap so an end to end connection is sufficient. On the other end using fibers implies adding electro-optic Tx/Rx but it's not necessarily true that this increases the overall cost of the IF link, provided that low cost Tx/Rx are found on the market. With this respect some market research and measurement have been performed at the Medicina laboratories, both on electronics devices and loose and tight fibers [9,10].
Frequency division multiplexing of the IF channels can be implemented by putting no more than two IFs on the same coaxial cable, otherwise higher channels should suffer strong attenuation and disequalization. This doesn't seem a solution in a coaxial frame, especially in view of a 50 feed array. The solution should be in the fibers frame, due to the larger bandwidth available and no disequalization problem.

6. REFERENCES

[1] S. Mariotti, A. Scalambra, A. Cremonini- Acceptance measurements on 32 GHz InP NRAO LNA for the ground receiver of the Cassini mission. IRA Int Memo.
[2] N. R. Erikson, R. M. Grosslein, S. Weinreb- A cryogenic focal plane array for 85-115 GHz using MMIC amplifiers
[3] M. Morgan, S. Weinreb – A monolithic HEMT diode balanced mixer for 100-140 GHz
[4] K. Chang, H. Wang, K. Tan, S. Bui, T. Chen, G. Dow, J. Bernez, T. Ton, D. Garske, T. Lin, L. Liu- a W-band monolithic downconverter
[5] C.J. Tarantella, Hittite Microwave Corporation- Ultra small mixers for K&Ka band communications
[6] S. Maas Non linear technologies
[7] S. Maas Microwave mixers
[8] A.Cremonini, E. Limiti, R. Nesti, A. Orfei, G. Tofani - 18-26 GHz cryogenic multifeed heterodyne receiver MMIC InP/GaAs based technologies – EuMw 2002, Milan Sep. 2002
[9] "Characterization of an analog low cost fiber optic link for radioastronomy applications". Degree thesis 2000-2001
[10] "Measurements of phase stability induced by temperature variation in loose and tight fibers". Degree thesis 2001-2002

7. PLANNED ACTIVITY FOR THE NEXT YEAR

-Measure and characterize the designed LNAs
-Provide a design, construct and characterize polarizer and omt
-Integration of the prototype receiver

8. LIST OF DELIVERABLES

-18-26GHz Feed horns
-Experimental characterization of the feed horn
-Dewar chamber for cryogenic receivers
-Experimental characterization of the dewar chamber

9. DISSEMINATION OF RESULTS

- A.Cremonini, E. Limiti, R. Nesti, A. Orfei, G. Tofani –
“18-26 GHz cryogenic multifeed heterodyne receiver MMIC InP/GaAs based technologies”
EuMw 2002, Milan Sep. 20

- G.G. Gentili, E. Martini, R. Nesti, G. Pelosi,
"Performance analysis of dual profile corrugated circular waveguide horns for radio astronomy applications,"
IEE Proc.-Microw. Antennas Propag.,l Vol. 148, No 2, April 2001